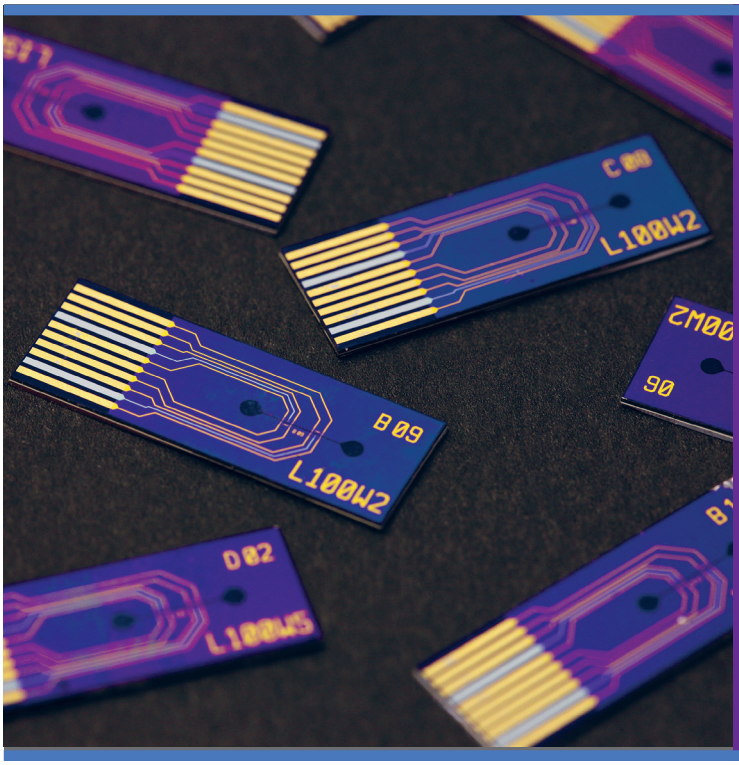
Novel Diagnostic Method for Personalized Treatment of Cancer

Zulfiqar, Azeem

Publication date:
2015

Document Version
Publisher's PDF, also known as Version of record



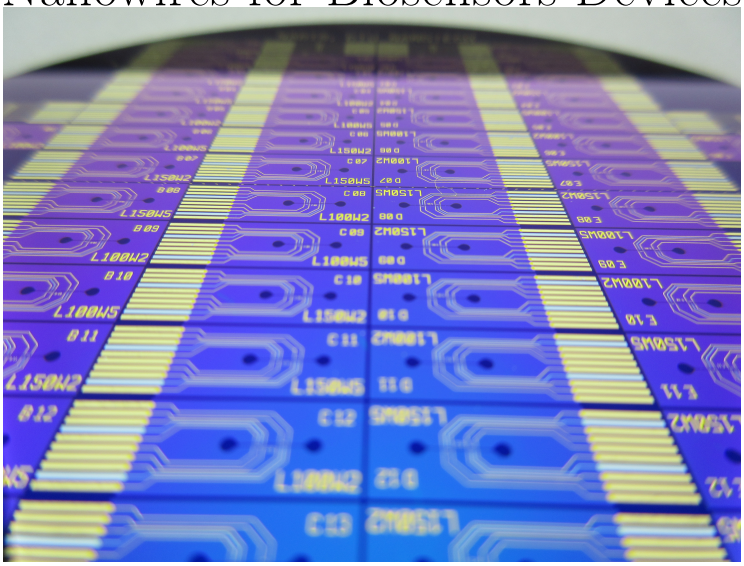
Novel diagnostic method for personalized treatment of cancer

Fabrication of Silicon Nanowires for Biosensors Devices

Azeem Zulfiqar
PhD Thesis August 2015

DTU Nanotech
Department of Micro- and Nanotechnology

Novel diagnostic method for personalized treatment of cancer:Fabrication of Silicon Nanowires for Biosensors Devices



Technical University of Denmark

Department of Micro-Nanotechnology

PhD Thesis

AZEEM ZULFIQAR

MAY 18, 2015

In the name of Allah, the most Beneficient, the most Merciful.

Abstract

Point-Of-Care (POC) devices, due to their better portability and easy-to-use functions, have already found their way into the domestic house hold appliances. The technologies developed for these devices have enabled the mankind to monitor the health related problems at home such as the blood pressure, glucose, hemoglobin, cholesterol level in the blood and many more. The efforts are now being made to develop a Point-Of-Care Technology (POCT) that can detect cancer at an early and potentially treatable stage. To fulfill this requirement, a highly sensitive sensing technology is needed that can detect very small amount of cancer markers in the blood drop to be used in a POC device.

Silicon Nanowires (SiNW) in a field effect setup have been demonstrated as a highly sensitive tool that can be used to detect very small amount of biomolecules. However, the manufacturing method to produce them relies on highly expensive tools e.g. e-beam lithography, and expensive substrates e.g. Silicon-On-Insulator (SOI) which poses hurdle in cheap and fast production of the devices that can be used for both research purposes and for domestic use.

In this project, a novel fabrication method, using in-situ doped polysilicon, has been developed for SiNW based devices that does not require the above mentioned expensive tools and resources thereby enabling faster and cost effective production of devices as compared to the already developed methods. In addition to this, the device has been made even more compact and portable by using a novel polyimide based technology to integrate microfluidics on top of SiNW sensor. Various generations of prototype devices have been used for bio-sensing experiments to detect antibodies and DNA hybridization that has shown very promising results and potential application of the device in clinical and patient level diagnostics.

In the first part of this thesis, the fabrication process of producing the SiNW based devices is explained in detail where three generations of the process are developed in order to obtain highly sensitive device. Different characterization techniques have been used to ensure better reproducibility and high throughput while keeping the sensitivity of the SiNW to a high level.

In the second part, the fabrication process to produce microfluidic channel on top of bio sensors by using polyimide is developed. The fabrication process to integrate closed-microfluidic system on top of SiNW is demonstrated. The durability of the microfluidic system has also been tested.

In the third part, different functionalization methods are explained and used to demonstrate the bio sensing on the SiNW sensor. The detection of cancer biomarker is also tested on these devices. Lastly, the alternative fabrication processes developed during this PhD project are discussed along with the problems faced during the development. These devices could not be tested due to time constraints.

Resumé (in Danish)

Point-of-Care (POC) systemer har allerede fundet vej ind i hospitalerne, praktiserende læger og endda private huse, på grund af deres bedre portabilitet og brugervenlighed. De teknologier, der er udviklet for disse systemer, har gjort det muligt for os at overvåge sundhedsrelaterede parametre i hjemmet, såsom blodtryk, glukose, hæmoglobin, kolesterol i blodet og mange flere. Der arbejdes nu på at udvikle en Point-of-Care Technology (POCT), der kan opdage kræft på et tidligt stadium, hvor den kan potentielt behandles. For at opfylde dette krav, er et meget følsomt sensor teknologi nødvendig, dvs. en teknologi, der kan påvise de meget små mængder af kræftmarkører i en dråbe blod, som er den mest almindelige patientprøve brugt til en POC system.

Silicium nanotråde (Silicon nanowires - SiNW), brugt som halvlederen i et felteffekt transistor konfiguration, er et meget følsomt værktøj, der kan anvendes til at detektere meget små mængder af biomolekyler. På nuværende tidspunkt er deres fremstillingsmetode for det meste afhængig af dyre værktøjer, f.eks. e-beam litografi, og dyre substrater, f.eks. Silicon-On-Insulator (SOI) substrater. Dette udgør en forhindring for den billige og hurtige fremstilling af de systemer, noget der er nødvendigt, hvis de skal anvendes i en POC system.

I dette projekt er en hidtil ukendt fremstillingsmetode for SiNW transistore udviklet, ved anvendelse af in situ doteret polysilicium. Metoden kræver ikke brug af de ovennævnte dyre værktøjer og ressourcer, hvilket betyder at den muliggør hurtigere og omkostningseffektiv produktion af denne type transistorer i forhold til de nuværende metoder. Udover dette er hele systemet blevet gjort endnu mere kompakt og transportabel ved hjælp af en ny polyimid-baseret teknologi, brugt til at integrere mikrofluidiske kanaler ovenpå den SiNW sensor. Forskellige generationer af prototyper er blevet anvendt til flere eksperimenter for at påvise deres funktion som sensorer, såsom målinger af antistoffer og detektion af DNA hybridisering. Disse har vist meget lovende resultater, og derfor demonstrerer den potentielle anvendelse af systemet til klinisk diagnostik på patient niveau.

I første del af denne afhandling forklares fabrikationsprocessen til fremstilling af SiNW-baserede systemer på et detaljeret niveau. Processen er udviklet i tre generationer med henblik på at opnå systemer med en høj grad af følsomhed. Forskellige karakteriserings-teknikker har været anvendt for at sikre en hurtig og robust proces, hvor følsomheden af de fremstillede SiNW holdes på et højt niveau. I anden del beskrives udviklingen af fabrikationsprocessen til dannelse af mikrofluid-kanaler på biosensorerne ved brug af polyimid. Det vises hvordan fabrikationsprocessen optimeres, og hvordan mikrofluid-systemet integreres med SiNW i et lukket-kanal design. Forskellige afprøvningsmetoder har været anvendt for at verificere mikrofluidsystemets bestandighed.

I tredje del vises hvordan SiNW overfladen modificeres for at muliggøre detektion

af biomolekyler. Forskellige funktionaliseringsmetoder forklares og anvendes til at demonstrere, at SiNW sensoren er i stand til at fungere som biosensor. Detektion af biomarkører for kræft afprøves også på disse systemer.

Til sidst diskuteres alternative fabrikationsprocesser udviklet i løbet af dette PhD projekt, herunder de i løbet af udviklingen konstaterede problemstillinger. Grundet tidsbegrænsninger kunne disse systemer ikke testes fuldt ud.

Acknowledgements

First and foremost I would like to thank Allah Almighty, Who gave me the strength and patience to bear with all the difficult times I have faced during this research project. The journey to this point, where I stand today was not at all easy and there were times when I used to pray to You, sitting alone in the lab, to guide me to the right path, the path of success.

I would like to express my special appreciation and thanks to my supervisor Associate Professor Winnie Edith Svendsen for giving me the opportunity to work on this project. I acknowledge the trust you have set on me and the freedom you gave me to try anything, at any time and at any cost to achieve the milestones set for the project.

Senior Researcher Maria Dimaki, my co-supervisor has played an important role in directing my research work to the present point. I would like to pay my deepest gratitude to her for paying attention to all the failures I had brought to her for discussion and for finding a way out to resolve the problems. She also helped me in correcting my first manuscript and my PhD thesis report.

Whenever I and my supervisors were stuck on fabrication related problems and no troubleshoots seemed to work, a small 'magical' advice from Professor Ole Hansen would always solve those problems. Though he was not my supervisor but he has always been very welcoming and ready to listen to my problems and provide me with the possible solution. Without his help it would not have been possible to achieve the good results in my research project.

In regards to microfluidics problem with polyimide I would like to thank Romen Rodriguez-Trujillo, post doc at NaBIS group who had helped me in the process development and characterization of polyimide and microfluidics testing. Thanks to PhD student Andrea Pfreundt for helping me in several aspects during my research project. Being the part of the same EU project she has helped me in analyzing data for bio-sensing experiments, setting up microfluidics pressure testing setup and teaching me the functionalization protocols. Moreover, writing the EU project reports and discussing project update presentations on every project meeting had really helped me to achieve the milestones in the project. François Patou PhD student had helped me in making electrical characterization of the devices. I would like to thank him also for providing useful suggestions to improve the fabrication process.

Thanks to Post doc Casper Hyttel Clausen who had helped me in correcting the LabVIEW program for electrical characterization, Post doc Karsten Brandt Andersen for transferring all the knowledge that NaBIS group had in silicon nanowires and to Post doc Dorota Kwasny for helping me with the DNA hybridization experiment.

I spent a good time as a Marie Curie fellow in the EU project EngCabra and I would like to thank all other fellows from partner institutes for all the good time we

had spent together as EngCabra fellows. I would also like to thank Paolo Livi and Amir Shadmani from ETHZ Basel for making the CMOS setup for my device and teaching me how to use it.

Danchip cleanroom staff has always been a great helping hand for me during the development of the fabrication processes. Whether it is the problem with the equipment or with my process, their immediate support has led me to achieve the good results in my research project. The lab technician Per Thor Jonassen has also helped me in setting up the microfluidics testing setup and how to do milling on the glass wafer. Without all their help and guidance I would not have achieved my targets.

A big thanks to my friends Saif-Ullah, Naveed, Aamir, Sarmad, Bilal, Qasim, Waseem and Fadil for their great company and relaxing chats during these three years of PhD life. The encouragement and motivation given from their side had always given me the strength to tackle with the research related problems in a relaxed way.

Lastly, I would also like to thank my parents who have struggled hard and sacrificed a lot to bring me to this stage. Their prayers and encouragement have kept me motivated in my career pursuits. My brother Salman and sister Shumaila have always been my support during my upbringing. I would also like to acknowledge the audacious support from my wife Samra throughout our relationship. She has played a pivotal in the compilation of my PhD thesis report. Without her involvement it would not have been possible to achieve this goal in my life. The prayers made by my parents-in-law, friends and relatives have always been a helping hand and source of motivation in my career endeavors.

$18^{th} May$ 2015

Azeem Zulfiqar

Contents

List of Figures

List of Tables

List of abbreviation

ALD	Atomic Layer Deposition
APTES	3-Aminopropyl-triethoxysilane
Bio-FET	Biological Field Effect Transistors
BSG	Boron Silicate Glass
CMOS	Complementary metal oxide semiconductor
DC	Direct current
DMSO	Dimethyl-Sulfo-oxide
DNA	Deoxyribonucleic acid
ssDNA	single-stranded Deoxyribonucleic acid
ncDNA	Non-complementary Deoxyribonucleic acid
cDNA	Complementary Deoxyribonucleic acid
DRIE	Deep Reactive Ion Etching
I_{DS}	Source-drain current
ICP	Inductively Coupled Plasma
ISFET	Ion Sensitive Field Effect Transistor
JFET	Junction Field Effect Transistor
LOD	Limit of detection
LPCVD	Low Pressure Chemical Deposition
MOSFET	Metal- Oxide Semiconductor Field Effect Transistor
NKG2D	Natural Killer Group 2D
NW	Nanowire
PBS	Phosphate buffered saline
PCB	Printed Circuit Board
PDMS	Poly-di-methyl-siloxane
PECVD	Plasma Enhanced Chemical Vapor Deposition
PI	Polyimide
PMMA	Poly-methyl meth-acrylate
POC	Point-of-care
POCT	Point-of-care testing
RF	Radio frequency
RIE	Reactive ion etching
RTA	Rapid thermal annealing
QCM	Quartz Crystal Microbalance
SEM	Scanning Electron Microscopy
SIMS	Secondary Ion Mass Spectroscopy
SiNW	Silicon nanowire
SOI	Silicon-On-Insulator
TEM	Tunneling Electron Microscopy
TEOS	Tetraethoxysilane
TMAH	Tetra-methyl-ammonium-hydroxide
ULBP2	UL16 binding protein 2
V_{DS}	Source-drain voltage
V_G	Back-gate voltage
VLS	Vapor-liquid-solid
ZIF	Zero-Insertion-Force
µTAS	Micro Total Analysis Systems

Chapter 1

Introduction

Since invention of the first ever biosensor in 1962 which was used to sense glucose by electrochemical sensing [1]. The field of biosensors has grown drastically and recent developments in nanotechnology have enabled us to produce miniaturized sensors, also known as nano-biosensors that require smaller amount of sample for bio-sensing [1, 2, 3, 4]. During the last few years, integration of these nano-biosensors with microfluidics has opened a new era of compact point-of-care (POC) devices that can play a major role in patient level diagnostics, personalized treatment, global health, drug development, food safety, and forensics [3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19]. According to American College of Pathology, POC testing (POCT) is defined as "tests designed to be used at or near the patient, that provide instant results, that do not require permanent dedicated space, and that are performed outside the clinical laboratories" [20].

This research project is part of the European Commission Marie Curie Networks for Initial Training (ITN) entitled "Engineering for Cancer and Brain diseases (EngCaBra)" involving 11 partners in total with medical, engineering and industry backgrounds. The broader aim of the project is to develop novel diagnostic methods and devices for early and reliable detection of cancer and brain diseases. Diagnosis of cancer at an early stage, in particular, is a compelling clinical need to allow efficient and personalized treatment decisions. Therefore, a highly sensitive and reliable detection method is required to address the gap.

The focus of this part of the project, carried out as my PhD thesis, is to design and fabricate silicon nanowire based biosensors with better yield and reproducibility. This biosensor has been demonstrated as a sensitive tool to detect very low concentration of biomolecules [21]. In addition to that the aim was to integrate the biosensor with a microfluidics system that can further be developed into POC device to be used as a tool to detect cancer from a drop of blood.

1.1 Point-Of-Care Testing for diagnostics

POC testing (POCT) has revolutionized the field of medical diagnostics by combining many advantages, such as fast processing, less sample handling, requirement of less sample material and reagents, affordability and ease of on-site detection [5, 13, 22, 23]. This technology has made its mark by significantly reducing the turnaround time as compared to conventional laboratory testing, from days and weeks to minutes and seconds figure 1.1, which is very important in clinical set-up for early

diagnosis, prescription of medication in the same visit to the doctor, monitoring the treatment etc.

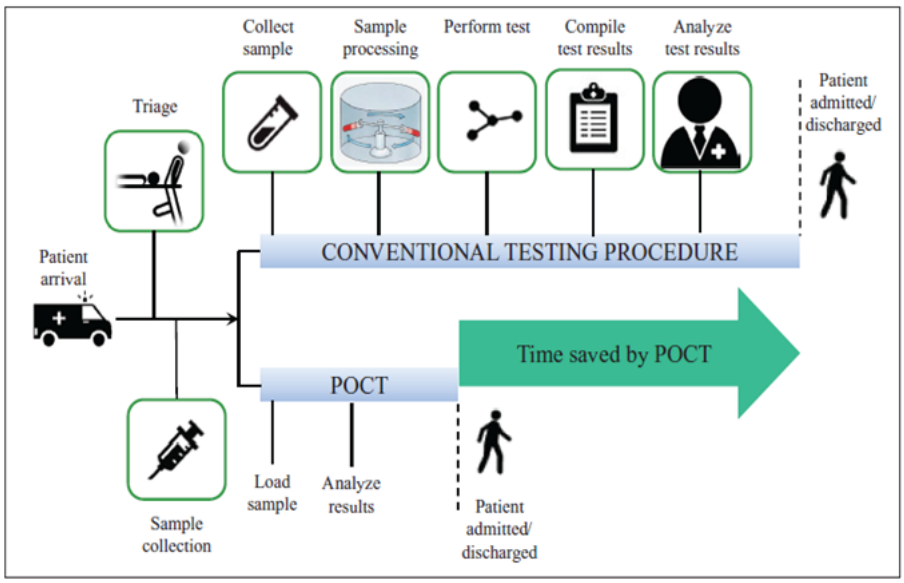


Figure 1.1: Turnaround time for results with point-of-care testing (POCT) compared to a conventional testing procedure [15]

POCT can also considerably reduce the economic burden in health care sector by offering ease-of-use at home so that patients can be monitored remotely for their health status thereby reducing the number of patients visiting health centres. Another advantage of POCT is its portability for onsite diagnosis that has been limited previously but has improved incredibly during last couple of years. A lot of design approaches are being implemented in microfluidic systems such as sample handling in biosensors without pumps/valves, the application of droplet-based microfluidics and paper-based microfluidic systems. These systems are used in lab-on-a-chip platforms, micro total analysis systems, and fluidic cartridges/ lateral flow (LF) strips. At the same time electronic read-out systems for biosensors with wireless communication ability and smart phone based interface are also developed [15, 16, 17, 24]. These POC devices can range in size from small chip to a table-top system [9].

The ideal design for a POCT device should include biosensor integrated with microfluidics in the system with an appropriate read out to allow automated processing of raw samples within the device, thereby requiring minimal operator training or intervention [25]. To achieve this, in this project, the design of the biosensor is made in such a way that it can easily be integrated with microfluidic system. Moreover, the fabrication method for the biosensor is carefully developed to keep the power consumption of the device to a low level. The goal in the end is to read-out the biosensor using smart phone based table top POC system.

1.2 Sensing with labels

The most common technique implemented in molecular- and microbiology for biosensing is the labeling of the molecules with fluorescent markers [26]. In this detection technique the target molecule is captured by the receptor (or specific anti-

body) molecule immobilized on the surface of the sensor followed by washing step to remove any unbounded molecules. After this step fluorescence labeled molecule, having binding affinity to the target molecule, is immobilized which then binds to the target-receptor (or target-antibody) complex. The fluorescence is observed on the sensor's surface by shinning laser (of specific wavelength) which confirms the success of the binding event. Thus the intensity of the fluorescence corresponds to the concentration of the target molecule in the sample. Figure 1.2 shows the schematic diagram of the detection steps by labeling molecules. The other variation in this technique can be done by conjugating the label to the target first and then immobilizing the target to the surface. In this case, the labelling can change the binding affinity of the target molecule, which can result in the variation of the analyte to the receptor coupling reaction [27]. The limit of detection (LOD), which is the measure of the lowest amount of the target biomolecule a sensor can sense, by this technique is in zepto mole range [28]. This technique is time consuming, laborious, expensive and requires more space which is a hurdle in the miniaturization of the biosensors and compact POC devices with integrated microfluidic and electrical read-out systems.

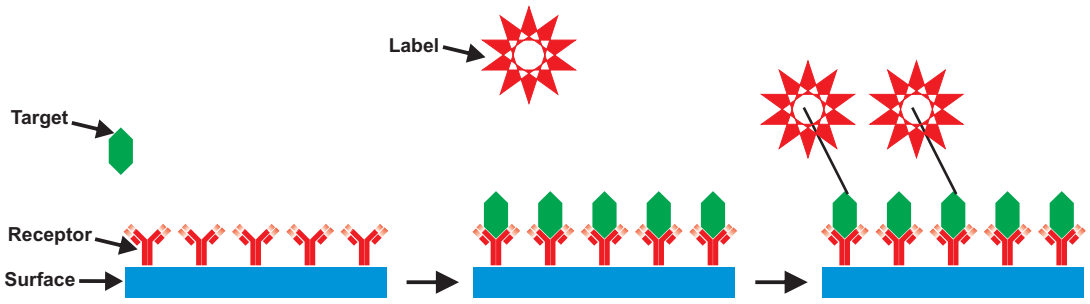


Figure 1.2: Schematic diagram of the detection process by labelling method

1.3 Label-Free Sensing

In label-free sensing, binding of the unlabeled target molecule to the sensor's surface changes the electrical behavior of the sensor e.g. resistance, capacitance etc. [29]. Label-free sensing technique has been proven to be the better alternative for biosensors with the ability to monitor real-time binding event of the analyte to the sensor's surface [30, 31]. The fact that the signal from the sensor can be read electronically enables the miniaturization of the sensor by integrating the sensor with the electronic read-out systems using modern CMOS (Complementary Metal Oxide Semiconductor) microelectronics fabrication techniques. There are several label-free sensing techniques that are used for bio-sensing purposes now-a-days e.g. piezoelectric , piezoresistive, redox potential and optical index based transducers. In this section the most common label-free sensors used for bio-sensing are discussed.

1.3.1 Quartz Crystal Microbalance Sensor

Quartz Crystal Microbalance (QCM) which has a mass-sensitive piezoelectric crystal with excitation electrode is commercially available label-free sensor [32]. It is

adapted to the liquid medium and gives a direct response signal in the form of change in the resonant frequency of the surface when the binding event occurs between a sensitive layer, grafted onto the surface of the transducer for specific analyte detection [33]. The LOD for QCM is $\sim$ 1ng [34, 32] which can be enhanced by higher frequency but then the signal to noise ratio goes down. QCM has been used for the detection of DNA, protein–ligand interactions, virus capsids, and bacterial and mammalian cells [15, 35].

1.3.2 Cantilever Sensor

Another transducer which is mostly used for label-free sensing is cantilever which has a piezoresistive component that translates the mechanical movement in the cantilever to the electrical signal. The detection principle is based on the change in the resonant frequency of the cantilever upon binding of the target analyte to its functionalized surface [36, 37]. The LOD for the cantilever is in the range of 1pg-1fg [38]. Cantilevers have been used to detect single virus, cancer biomarkers and nanoparticles in fluid [30, 38, 39].

1.3.3 Amperometric Sensor

Amperometric biosensors measure the change in electric current due to redox reactions that occur upon interaction of electroactive biomolecules on the surface of the biosensor. It consists of a working electrode covered by a bio-recognition layer (a thin layer of enzymes) that catalyzes the redox reaction on top of the electrode surface thereby generating reactive by-products and releasing electrons that can be measured in form of a current through the working electrode. This technique has been used to sense glucose, lactate [40], pesticides and nerve agents [41].

The sensitivity of any label-free sensor depends on the kinetics of the binding reaction i.e. strength of the binding between the target and receptor molecule. It can also be referred as the slope of the response curve [42] of the binding event. The current limitation of the label-free sensors lies in the non-specific binding of the biomolecules to the surface which needs improvement in probe immobilization chemistries. So far, there is no single agreed method to compare the LOD or sensitivity of different label-free sensors based on the published results [31].

1.4 Silicon Nanowire Label-Free Sensor

The silicon nanowire (SiNW) in a field effect setup, where biological sample acts as gate, is used as a label-free sensor that is termed as Bio-FET sensor hereafter. The factors that are considered important for this project include its low cost, high sensitivity, reduced size as a biosensor, possibility of integration with microfluidics and CMOS read-out system for real-time monitoring of the binding event along with its development towards compact POC device with smart phone display and control system.

1.4.1 Sensing Principle

SiNW Bio-FET sensor operates as a potentiometric sensor which means that the charged chemical or biomolecules bound to the surface of the SiNW can influence the charge carrier distribution in the conducting channel of the SiNW. The factors that make it highly sensitive are the high surface to volume ratio and its size, especially radius, which are comparable to the biological species. Figure 1.3 shows the schematic of the biomolecule sensing using p-type SiNW. The detailed theory along with the limitations of this sensor is discussed in Chapter 2.

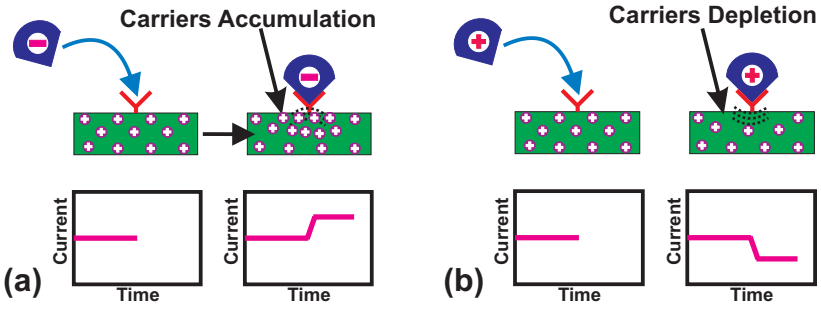


Figure 1.3: Schematic diagram of the sensing principle using p-type SiNW. The target molecule with a certain charge binds to the receptor immobilized on the sensor's surface which changes the charge distribution in SiNW

1.5 State of the art

The first demonstration of SiNW as label-free sensor was made by Yi Cui et al from Charles Lieber's research group where they detected streptavidin (target molecule) by functionalizing the SiNW with biotin (receptor). They were able to detect the concentration of streptavidin down to 10pM in real time measurements [43]. They also tested reversible protein reaction on biotin functionalized surface by immobilizing monoclonal antibody against biotin (m-biotin). A change in signal was observed due to binding of m-biotin to the surface. The m-biotin was removed by using pure buffer solution which again resulted back to the original conductance in the SiNW. In addition to that, they also demonstrated the pH sensing by using solutions of different pH values on the functionalized SiNW with 3-Aminopropyltriethoxysilane (APTES). Figure 1.4 shows the results from Yui et al demonstrating real time detection of reversible protein and pH sensing. Later on, the SiNWs fabricated by them using bottom-up method (explained in the next section) were used for successful detection of DNA [44],virus [21], and cancer detection by multiplexing [45]. However, the fabrication method of SiNW developed by the fore-mentioned research group was complex and was later improved by various other research groups who developed different fabrication processes by using Silicon-On-Insulator (SOI) wafers [46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57] and polysilicon [58, 59, 60, 61, 62] with demonstration of successful bio-sensing.

In the section below the most commonly used techniques for fabrication of SiNW Bio-FET sensor, developed over the years, are explained.

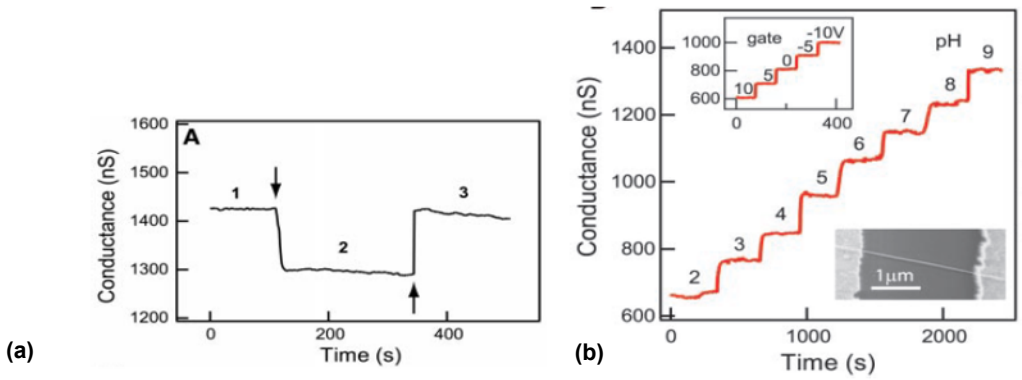


Figure 1.4: Real-time detection of reversible protein binding (a) Plot of conductance versus time for a biotin-modified SiNW, where region 1 corresponds to buffer solution, region 2 corresponds to the addition of 3 µM m-antibiotin antibody (460 µg/ml), and region 3 corresponds to flow of pure buffer solution (b) Real-time detection of the conductance for an APTES modified SiNW for pHs from 2 to 9; the pH values are indicated on the conductance plot (inset top). Plot of the time-dependent conductance of a SiNW FET as a function of the back-gate voltage (inset bottom). Field-emission scanning electron microscopy image of a typical SiNW device [43].

1.6 Fabrication Techniques

The fabrication of the SiNW can be divided into two main categories i.e. bottom up fabrication and top down fabrication.

1.6.1 Bottom up fabrication

This technique has been adopted by the Charles Lieber's research group where they have used vapor-liquid-solid (VLS) process to grow SiNW on the substrate[59]. The gold particles are first adsorbed on the substrate which is then transferred into the furnace where the mixture of silane (SiH_4), diborane (B_2H_6) and argon (Ar) gases is released at 460℃. This furnace process results in the growth of p-type SiNW grown in the random directions and the diameter of the SiNW is set by the size of gold particle adsorbed on the substrate. This step is followed by Scanning Electron Microscopy (SEM) and Tunneling Electron Microscopy (TEM) inspection of the SiNWs. Figure 1.5 shows the schematic diagram of this process. The next step is

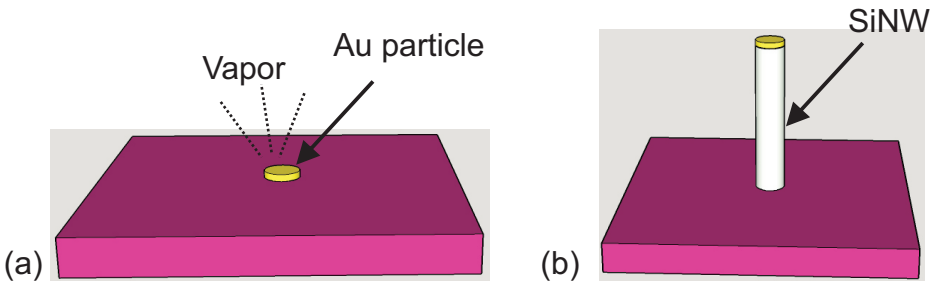


Figure 1.5: Schematic diagram of SiNW growth using Vapor-Liquid-Solid process

sonication in ethanol solution which releases the SiNW from the substrate and makes the solution containing free standing SiNW. Another substrate with insulator on top

is then patterned with electrodes made in Chromium and Gold followed by SiNW solution dispensation and alignment by Langmuir-Blodgett process. The passivation of the electrodes is done by Plasma Enhanced Chemical Vapor Deposition (PECVD). Figure 1.6 shows the images during fabrication process. The main advantage of this

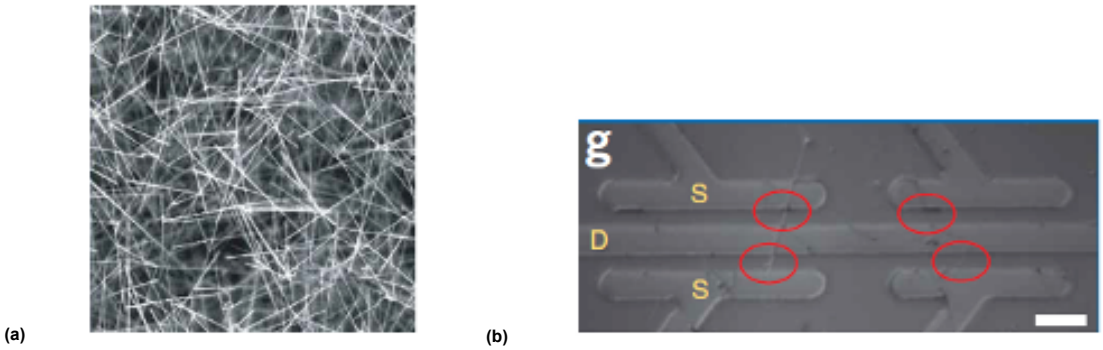


Figure 1.6: (a) SEM Image of grown SiNW (b) highlighted red circles indicate the positions of SiNWs between source and drain electrodes [Taken from [63]

technique is that the radius of the SiNW can be adjusted by changing the size of the Au particle that can influence the sensitivity of the biosensor. However, the process has various limitations including comparatively low yield, batch to batch variation, and moderate to poor reproducibility of the SiNW patterning. In addition to this, the process is time consuming and involves several inspection steps.

1.6.2 Top down fabrication

The top down fabrication of SiNW Bio-FET devices is based on the standard semiconductor processing steps where the patterning techniques like e-beam, deep UV lithography followed by dry or wet etching are commonly used, and the source-drain contacts are made by e-beam evaporation technique.

1.6.2.1 Fabrication by e-beam lithography

In this technique the SOI wafer with thin device layer, in the range of 100 nm, is used as the substrate. The first step is to grow silicon dioxide (SiO_2) on top of it by dry oxidation process which reduces the thickness of silicon to 40-50 nm. The source drain contacts are ion-implanted to form ohmic contacts after metal depostion. The e-beam lithography is done on top of PMMA (PolyMethyl MethAcrylate) which is used to pattern Chromium after lift-off process. The Cr serves as a mask to pattern SiO_2 by dry etching. After removing Cr SiNW are patterned by dry etching. The metal contacts are formed later by lift-off process followed by passivation [51] figure 1.7 This process provides higher yield and better reproducibility in comparison to bottom up fabrication technique but at the same time, the cost of producing the devices is raised due to use of expensive SOI wafer and e-beam lithography.

1.6.2.2 Fabrication by Nano-imprint lithography

In this technique, SOI wafers are used with device layer thickness of around 360 nm. The thickness of device layer is reduced by wet oxidation followed by removal

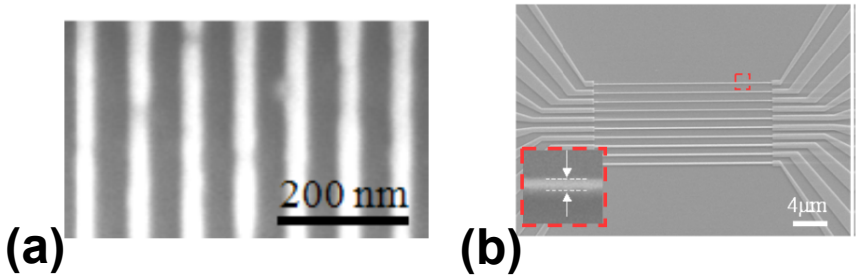


Figure 1.7: SEM image of SiNWs (a) linewidth (LW) and line edge roughness (LER) of silicon nanowires fabricated by the top-down nanofabrication process (electron beam lithography and reactive ion etching of the silicon on insulator substrate) (b) silicon nanowire sensor arrays fabricated by the top-down nanofabrication process (inset: 50 nm width) Taken from [51]

of oxide by wet etch. As a next step, thin dry oxide is grown on top of silicon that will be used later as a mask for patterning SiNW. In the meantime, a nano-imprint mold is prepared on a separate Si wafer by using e-beam lithography made by using PMMA resist and dry etching. This mold is then used to make the pattern of thin resist on top of SiO_2 of the SOI wafer followed by wet etch of silicon in Tetramethylammonium hydroxide (TMAH) which produces trapezoidal shaped SiNW. The source and drain are also ion-implanted with high dose to form ohmic contact with the metal electrodes. The fabrication steps are shown in Figure1.8 along with the SEM image after fabrication [64] This fabrication technique also provides high yield

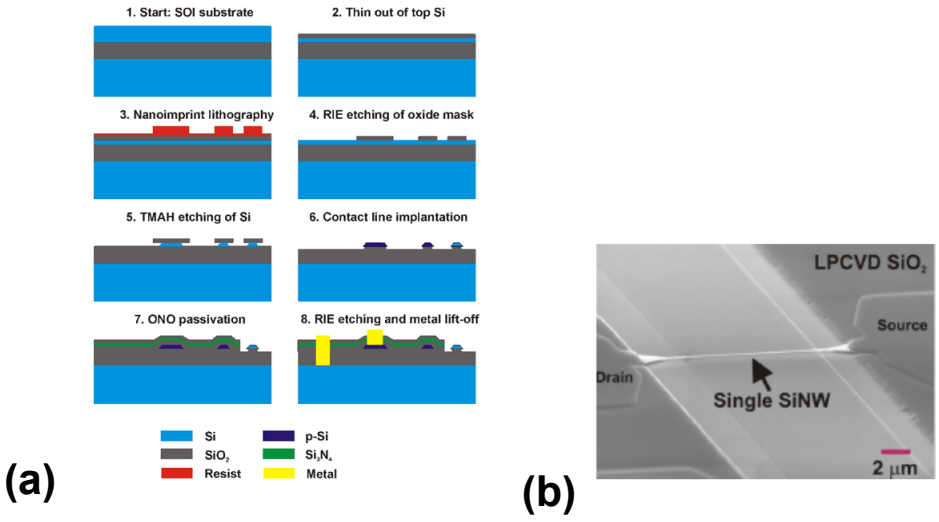


Figure 1.8: (a) Schematic of fabrication steps SiNW Bio-FET (b) SEM images of a single SiNW taken from [64]

and reproducibility. The advantage of this technique is that the time of fabrication is reduced by making the nano-imprint mold once which facilitates the lithography process by skipping e-beam lithography on each wafer. However, this process is also dependent on the SOI wafers and is therefore as expensive as e-beam lithography.

Similarly, spacer fabrication technique [58] for patterning SiNW also offers advantages by avoiding expensive e-beam lithography technique while maintaining the

high yield and reproducibility. This technique also uses ion-implantation of source-drain. However, to achieve this fabrication method, several steps are added in the process which increases the cost and fabrication time.

1.7 Project Goal and Approach

The main goal of this project is to develop a top-down fabrication process for a SiNW Bio-FET by using in-situ doped polysilicon to form the nanowires. The FET is to be operated in a junction-less setup. The aim is to be able to fully deplete the nanowire by a low externally applied potential, as is also demonstrated by other fabrication methods. Further the goal is to be able to achieve a sensor sensitivity similar to that achieved by nanowires made by crystalline silicon and with conventional fabrication processes. In addition to this, the fabrication process is developed in a way to ensure the production of the sensor with low-cost, robust, high yield and reproducibility. The integration of a microfluidic system is also studied in this project which can enable us to use the sensor in a POC device setup.

To achieve these goals, different generations of fabrication processes are developed and tested. To keep the process simple, standard UV lithography is used followed by wet etch patterning of SiNW which enable batch process of several wafers at a time. Since the polysilicon is doped already, the expensive ion-implantation step is also omitted from the fabrication process. For microfluidic channel, polyimide has been studied as a potential candidate that has compatibility with the microelectronics fabrication process thus enabling the sensor's integration with CMOS read-out systems.

1.8 Organization of the thesis

This thesis is divided into nine chapters and four appendices.

The second chapter gives the theoretical background of the field effect transistor (FET) in the beginning, followed by the SiNW Bio-FET sensors along with its characteristics. In addition to this, the limitations of the SiNW Bio-FET sensor are also discussed in detail. In the last part, different electrical characterization techniques are explained that can be used to determine the main characteristics of the SiNW Bio-FET sensor.

In the third chapter, three generations of fabrication processes that are developed during this project, by using in-situ doped polysilicon, are explained. Different characterization techniques are also discussed that are used to determine the reproducibility and yield of the process.

In the forth chapter, a detailed study on polyimide as a microfluidic channel is done. The patterning method, optimization of etching recipes, forming a closed-channel microfluidics along with the bond strength tests done for the durability of the channels are explained. It is also compared to the SU-8 polymer that is commonly used as microfluidic channel.

The fifth chapter gives the glimpse of different measurement setups that are used for various bio-sensing experiments and electrical characterization of SiNW Bio-FET sensor.

In the sixth chapter, the characterization made by secondary ion mass spectroscopy and the electrical characterization of the devices made by all the three generation processes are explained and discussed. The electrical measurements done during each step of the fabrication process to ensure better reproducibility and yield are also explained in detail.

In chapter seven, different functionalization methods used to modify the surface of SiNW to increase the affinity towards target molecules are explained in detail, followed by description of bio-sensing experiments, for DNA hybridization, two antibody system, and NKG2D cancer biomarker detection, along with the results and their discussions. In the last part, pH measurements made on the 3rd generation device is discussed followed by the liquid gate measurements of the device.

In chapter eight, two other fabrication processes developed during this project are discussed and explained in detail. The problems faced during the processes and the reasons for discontinuing them are also explained.

In the final chapter, the conclusions drawn on the basis of this work along with future work and prospectives are discussed.

Chapter 2

Theory

This chapter starts with the description of the working principle of a field effect transistor (FET) and its important characteristics as the sensing principle of silicon nanowire (SiNW) Bio-FET sensor is inspired by the FET devices. The theory involved in SiNW Bio-FET along with the limitations in the sensitivity of the biosensor is discussed later. Methods to extract the transfer characteristics of the Bio-FET device are explained in the last part of the chapter.

2.1 Field Effect Transistor

A semiconductor device in which the operational current is controlled by an electric field is called Field effect transistor (FET) [65]. It is also known as a 'unipolar device' which means that only one type of charge carriers is involved in the conduction process [65, 66]. The FET device consists of three terminals i.e. source, drain and gate whereby the operational current flows between source and drain through a channel which is controlled by a gate potential. The FET devices are used in several configurations e.g. Junction Field Effect Transistor (JFET), Metal- Oxide Semiconductor Field Effect Transistor (MOSFET), Ion Sensitive Field Effect Transistor (ISFET) etc. Figure 2.1 shows a schematic diagram of a metal-oxide semiconductor field effect transistor (MOSFET).

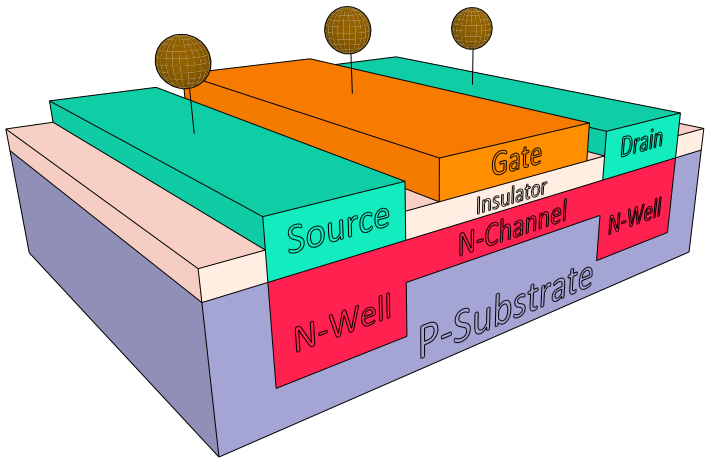


Figure 2.1: Schematic diagram of a MOSFET device

2.1.1 FET Operation

In the FET device (shown in figure 2.1) when a positive gate voltage is applied, an electric field is formed between the gate and the substrate with insulator in between. Due to capacitive behavior the positive charges from the gate terminal will attract the negative charges available at the substrate's N-wells which leads to the formation of the N-channel between the wells and the operational current starts flowing from source to drain via the N-channel, which enhances the conductivity of the device. Similarly, if a negative gate voltage is applied on the gate, the n-channel can be closed and this will reduce the conductivity of the device.

2.1.1.1 Analogy

This concept can be well understood by keeping in mind the example of the water valve shown in Figure 2.2. In this example the valve acts like a gate terminal which controls the flow of water from source to drain.

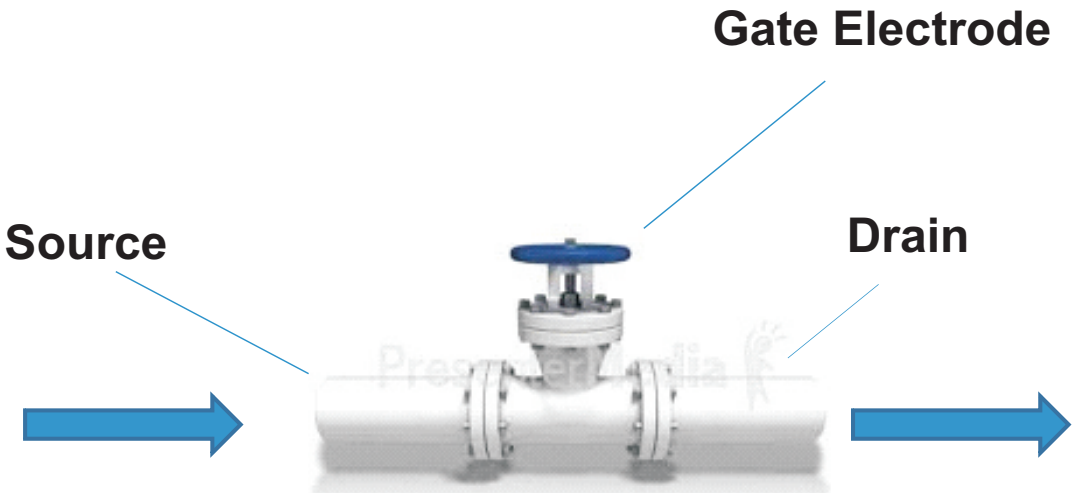


Figure 2.2: Schematic diagram of a water valve system

2.1.2 FET Characteristics

2.1.2.1 Mobility

When an electric field is applied through the gate terminal, the holes and electrons are forced to move in one direction. The term mobility is used to express how good the movement of holes and electrons will be in the device [67, page 173]. Higher mobility value means that the charge carriers will face less resistance and vice versa. While moving, the charged particles collide with the different atoms in the crystal which makes them scatter and lose their energy. Throughout this process, the particle acquires an average drift velocity, ν_{dp} which can be expressed as

$$\nu_{dp} = \mu_p E \tag{2.1}$$

where μ_p is the constant of proportionality and is called the hole mobility (for positively charged particles) and E is the electric field applied [67, page 155].

The net movement of the charges due to electric field is called drift current which is written as

$J_{drf} = Q\nu_d$

Where Q is the volume charge density and ν_d is the total drift velocity. As both the electrons and the holes are involved in the drift current, the total drift current density can be written as

$$J_{drf} = Q(\nu_{dp} + \nu_{dn}) \tag{2.2}$$

$$J_{drf} = Q(\mu_p E + \mu_n E) \tag{2.3}$$

If p is the concentration of holes and n is the concentration of electrons then

$Q = ep$ for holes and $Q = en$ for electrons. Therefore the above equation can be written as

$$J_{drf} = e(\mu_p + \mu_n)E \tag{2.4}$$

Which gives the conductivity as

$$\sigma = e(\mu_p p + \mu_n n) \tag{2.5}$$

2.1.2.2 Accumulation mode

The MOSFET is said to be in accumulation mode when a positive gate voltage is applied to the gate terminal and electrons flow from source to drain in the n-channel. Increasing the positive potential will increase the channel size and thus the conductivity.

2.1.2.3 Depletion Mode

The depletion mode is achieved when a negative gate voltage is applied to the gate terminal. Increasing the negative potential will decrease the channel size and also the conductivity and will ultimately close the channel.

2.1.2.4 Threshold Voltage

If the negative bias is increased beyond depletion mode then a strong electron inversion layer is formed. This applied voltage required to achieve the inversion point is called threshold voltage [67, page 465].

2.1.2.5 Sub-threshold region

When the gate voltage is below the threshold voltage and the device is weakly inverted, the corresponding source-drain current is called the subthreshold current.

2.1.2.6 Transconductance

The change in the source drain current with respect to the corresponding change in gate voltage is known as transconductance g_m of the FET device and it can be written as

$$g_m = \partial I_D / \partial V_G \tag{2.6}$$

Where ∂I_D is the change in source drain current and ∂V_G is the change in gate voltage [67, page 498]

2.2 Silicon Nanowire Biological-Field Effect Transistor (Bio-FET)

In silicon nanowire (SiNW) based Bio-FET device, shown in figure 2.3, the source, drain and the channel are doped with the same type of dopants i.e. p-type in this case. This means that the device is always turned on with the silicon nanowire acting like a resistor with low dopant concentration whereas, the source and the drain are highly doped to have a good ohmic contact with the metal electrodes.

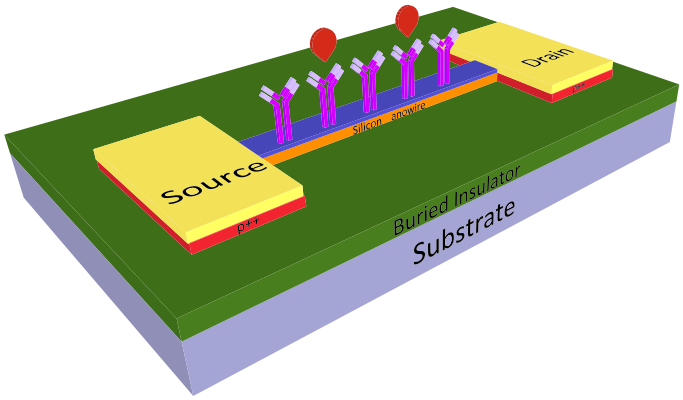


Figure 2.3: Schematic diagram of a SiNW Bio-FET device with functionalization layer and analyte immobilization

The SiNWs are patterned on top of a buried insulator to avoid any current leakage from source, drain and nanowire into the substrate.

2.2.1 Sensing Principle

The top oxide surface of the SiNW is modified chemically to form a layer of receptors; this process is called functionalization. When an analyte of interest is released on the BioFET device these receptors due to their binding affinity with the target analyte catch them which results in the change of the charge concentration on the surface of the functionalized SiNW. The charge concentration on top of the SiNW acts like a gate and modulates the source-drain current.

2.2.1.1 Sensitivity of SiNW Bio-FET

The sensitivity of the SiNW is written as

$$S = \frac{G_{after} - G_{before}}{G_{before}} = \frac{\Delta G}{G_0} \tag{2.7}$$

Where G_0 is the conductance of the SiNW before the immobilization of the analyte on the SiNW and ΔG is the change in the conductance after the analyte is immobilized.

The conductance of the SiNW is mainly dependent on the source-drain current I_{DS}. The surface charge density of the analyte (Q_{BIO}) present on the top of SiNW controls the charge carrier density in the SiNW (Q_{SINW}) which means that

$$Q_{BIO} = Q_{SINW} \tag{2.8}$$

Theoretically the above mentioned equation should work very well, but experimentally there are two main factors that influence the conductivity of the SiNW during measurements and affect the authenticity of the results:

1. Some part of the analyte charge is screened in the electrolyte in which it is present. This effect can be modelled using the Debye-Huckel theory, and results in the calculation of the so-called Debye screening length.

2. There is also charge screening within nanowire due to presence of oppositely charged carriers. This can be modelled by introducing the so-called Thomas-Fermi screening length. Both lengths are explained in detail below.

2.2.1.2 Debye Screen Length

According to this theory, when a charged surface is immersed in an electrolytic solution, it affects the charge distribution in the solution. In the case of a Bio-FET device, most of the analyte biomolecules are found in an electrolyte solution e.g. phosphate buffered saline (PBS). When the analyte with a certain charge is immobilized on the surface of the SiNW, the ions in the electrolyte that are oppositely charged to the analyte (also called counter ions) will be attracted to the surface of the analyte due to electrostatic forces, which results in the false projection of the analyte charge density on the SiNW. Similarly the charged ions in the electrolyte that have the same charge as that of the analyte, also known as co-ions, will be pushed away from the biomolecules. This will result in the non-uniform distribution of counter ions near the surface of the SiNW where the biomolecules are present and far away from the surface the charge neutrality is achieved by uniform distribution of both the counter ions and co-ions [68, page 108]. This redistribution of the ions in the solution lead to the formation of an Electric Double Layer, where one layer is the surface charge of the biomolecules spread all over the surface of the top oxide of SiNW and the second layer consists of ions distributed around biomolecules surface. The figure 2.4 shows the distribution curve of ions perpendicular to the charged surface. This ionic charge distribution can be mathematically expressed by Boltzmann equation equation

$$\rho_x = \rho_\infty \exp(\frac{-ze\psi_x}{kT}) \tag{2.9}$$

Where x is the distance from the surface, ρ_x is the surface charge density at a distance x and ρ_∞ is the bulk concentration of the electrolyte with uniform ionic distribution, z is the valency of the electrolyte, ψ is the electrostatic potential, k is the Boltzmann constant and T is the temperature [69, page 231]. Similarly, the ionic concentration of counter-ions and co-ions can be written as

$$n_i = n_{i\infty} \exp(\frac{-z_i e\psi}{kT}) \tag{2.10}$$

Where $n_{i\infty}$ is the ionic number concentration at neutral state, n_i is the ionic number of the ionic species (counter ions or co-ions) [68, page 110].

To better understand the effect of the counter ions on the SiNW response, the surface potential on top of the silicon oxide needs to be calculated. This will be influencing the source-drain current in the SiNW. This can be done by assuming that the surface of the SiNW is a planar one, which will enable us to treat this as an one dimensional problem.

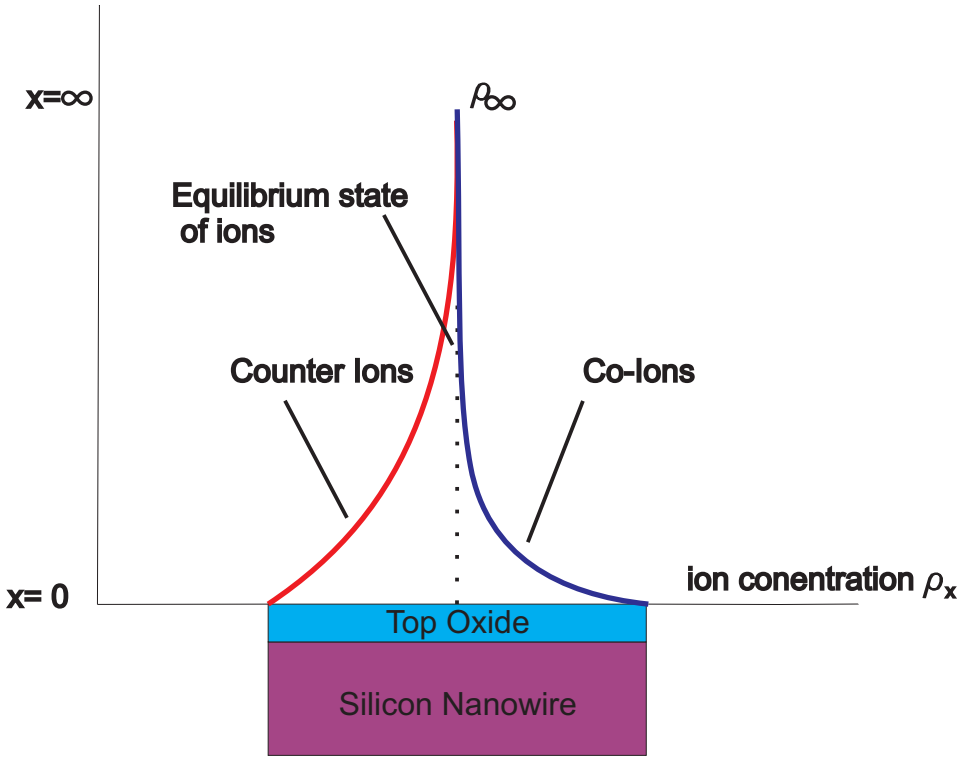


Figure 2.4: Ion distribution perpendicular to the charged surface. Near the oxide surface the counter-ions are accumulated and co-ions are depleted. The charge neutrality is achieved in the bulk electrolye concentration, $x = \infty$ (inspired by [69, page 232]

Based on the above facts, the potential distribution within the electrolyte due to electric double layer can be seen in figure 2.5 According to Poisson equation for planar surface the potential distribution can be written as [68, page 112]

$$\nabla^2\psi = -\frac{\rho_{DL}}{\epsilon\epsilon_0} \tag{2.11}$$

Where ρ_{DL} is the net charge density of the electric double layer and can be written as

$$\rho_{DL} = ze(n_+ - n_-) \tag{2.12}$$

ϵ is the dielectric constant of the solution and ϵ_0 is the permittivity of the free space.

To facilitate the solution, a symmetric electrolyte (1:1) is considered. Therefore, by using the boundary conditions shown in the above figure we can get Poisson-Boltzmann equation

$$\nabla^2\psi = -\frac{2zen_\infty}{\epsilon\epsilon_0} sinh(\frac{ze\psi}{kT}) \tag{2.13}$$

According to the Gouy-Chapman theory the solution to this equation [68, page 114] is

$$\psi = 2ln(\frac{1+\gamma\exp(-kx)}{1-\gamma\exp(-kx)}) \tag{2.14}$$

where $\gamma = tanh(\psi_s/4)$ and $k^{-1} = \sqrt{\frac{\epsilon\epsilon_0 kT}{2z^2e^2n_\infty}}$ k^{-1} is called Debye Length [68, page 114] which is a measure of the thickness of the electric double layer, the Debye's length will be denoted by L_D hereafter.

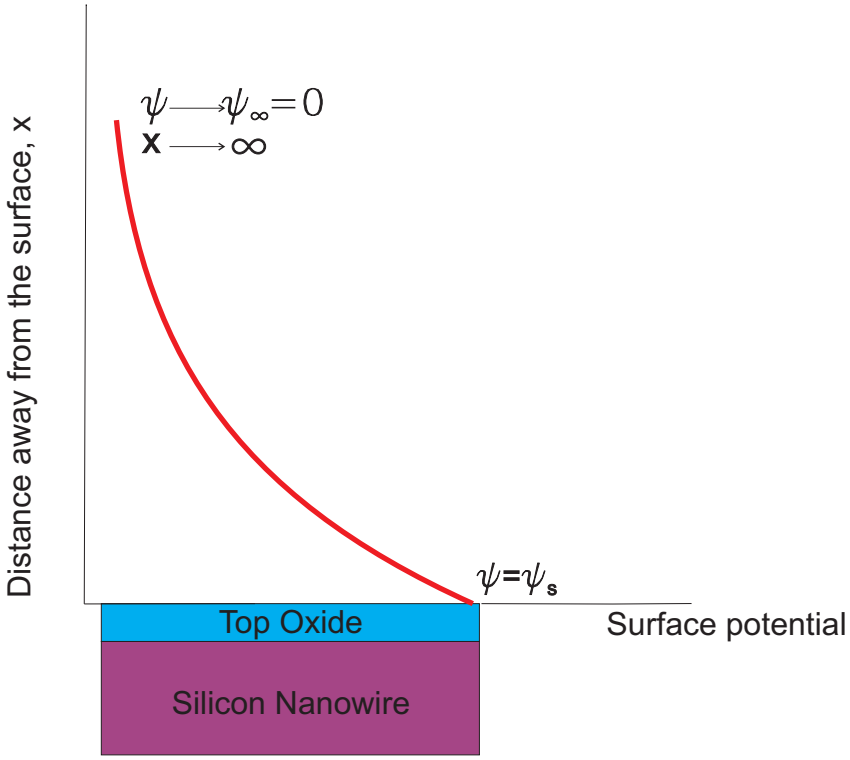


Figure 2.5: Potential distribution over the Top oxide surface (inspired by [68, page 112])

When the surface potential is very small e.g. the electrolyte's concentration is very small then the term

$$sinh(ze\psi/kT) \approx (ze\psi/kT) \tag{2.15}$$

By using the Debye-Huckel approximation, the solution to the Poisson-Boltzmann equation [68, page 116] [69, page 239] will give us

$$\psi(x) = \psi_0 \exp(-kx) \tag{2.16}$$

To estimate how much of the analyte's charge will be screened by the electrolyte, we can calculate the centroid charge or the effective charge of the electric double layer by normalizing the surface charge densities.

$$< x > = \frac{\int_0^\infty x\rho_{DL}(x)dx}{\int_0^\infty \rho_{DL}(x)dx} \tag{2.17}$$

From Poisson's equation mentioned before and using all the approximations

$$\rho_{DL} = -\frac{z^2e^2}{\epsilon\epsilon_0 kT}\psi_0 \exp(-kx) \tag{2.18}$$

By putting this value in equation above we get the centroid as follows

$$< x > = k^{-1} = L_D \tag{2.19}$$

So we can say that there is another capacitor next to the SiNW and the distance of the electrode is one Debye length away, as depicted in figure 2.6: The capacitance

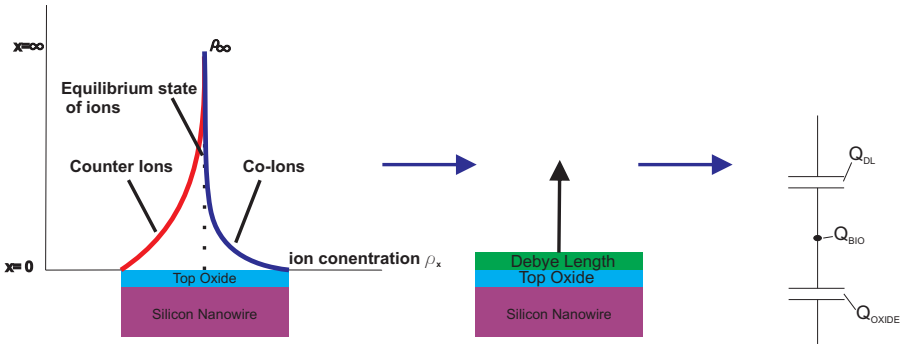


Figure 2.6: Simplification of electric double layer case. The electric double layer acts like another capacitor which is one debye length away from the SiNW.

of this layer is

$$C_{DL} = \frac{\epsilon\epsilon_0}{k^{-1}} = \frac{\epsilon\epsilon_0}{L_D} \tag{2.20}$$

So, for Bio-FET the analyte charge (Q_{BIO}) will be divided into two capacitors connected in series.

$$Q_{BIO} = Q_{DL} + Q_{oxide} \tag{2.21}$$

Where Q_{DL} is the charge screened by the electric double layer and $Q_{oxide}$is the charge across top oxide of SiNW.

Hence, the sensitivity of the SiNW Bio-FET is directly influenced by the Debye-Screening Length which changes by the change of the electrolyte ionic concentration.

2.2.1.3 Thomas-Fermi Length

According to this theory, the sensitivity of SiNW is also influenced by the screening of the charges within the semiconductor nanowire. Consider that the Bio-FET device is made of p-doped SiNW where the holes are the majority carriers. These holes will interact with each other by Coulomb forces, which means that they will repel each other within the nanowire. The electrons in the vicinity of these holes will get attracted to the positively charged particles and reduce their field effect. To understand the interaction, we have to consider two electrostatic potentials. One of them is due to the holes also known as external potential ϕ^{ext} and the other is the total potential produced by holes and the screening electrons also known as induced potential ϕ^{ind} [70]

$$\phi = \phi^{ext} + \phi^{ind} \tag{2.22}$$

There are several approximations to calculate the electron charge density that can give us the total potential. One of the most precise approximations is called Thomas-Fermi approximation which has been implemented to calculate the screening length in SiNW by several research groups. The screening length for a p-doped SiNW is written as

$$\lambda_{TF} = \sqrt{\frac{\hbar^2 \epsilon \pi^{4/3}}{m^* e^2 p_0^{1/3}}} \tag{2.23}$$

Where $\epsilon_s i$ is the permittivity of silicon, m^* is the effective mass of the charge and p_0 is the charge carrier concentration [71]. For hole density of around 10^{18} – 10^{19} atoms/cm^3, the screening length is around 1-2 nm which means that the analyte's

charge on the surface of SiNW can only gate within a surface thickness of around 1-2 nm [72].

2.3 Bio-sensing with Bio-FET

The response of the SiNW Bio-FET upon binding of the analyte can be approximated if we know the type of majority charge carriers in the SiNW and the net charge of the analyte. For example, if we have a p-type SiNW (with positive charges being the majority carriers) then the response of the Bio-FET can be estimated as shown in 2.7. When a negatively charged analyte is captured by the receptors over

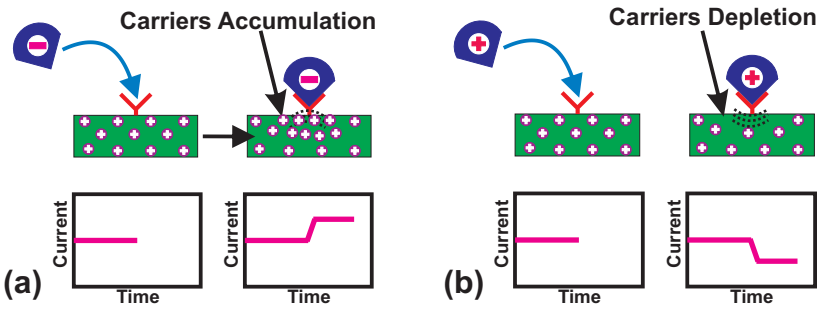


Figure 2.7: For a p-type SiNW (a) Negatively charged analyte increases the conductivity (b) Positively charged analyte decreases the conductivity

the SiNW due to electrostatic forces, the positively charged carriers within the SiNW will be attracted towards the surface that result in increased flow of current from source to drain. On the contrary, when the analyte with positive charge is added on the surface of the SiNW it repels the positive charged carriers away from the surface of the SiNW thus resulting in the reduced current flow from source to drain.

2.4 Characterization Theory

The main characteristics of the FET devices are explained in section 2.1. In this section, the characterization method of p-type SiNW Bio-FET is discussed in detail. After the fabrication of the SiNW Bio-FET devices, these are characterized in terms of their electrical properties, before application into biological assays. The electric characterization is done by using an electrical measurement setup shown in figure 2.8.

2.4.1 Mobility

The first step is to observe the resistance of the nanowire (NW) at different gate voltages, which will assure us that the NW can be gated by an external electrical field. figure 2.9 below shows the change in source-drain current I_{DS} when plotted against drain-source voltage at different gate potentials. This shows that it is possible to model it as a resistor; then according to ohm's law the source-drain current I_{DS} for this linear regime can be written as

$$I_{DS} = \frac{V_{DS}}{R_{SINW}} \tag{2.24}$$

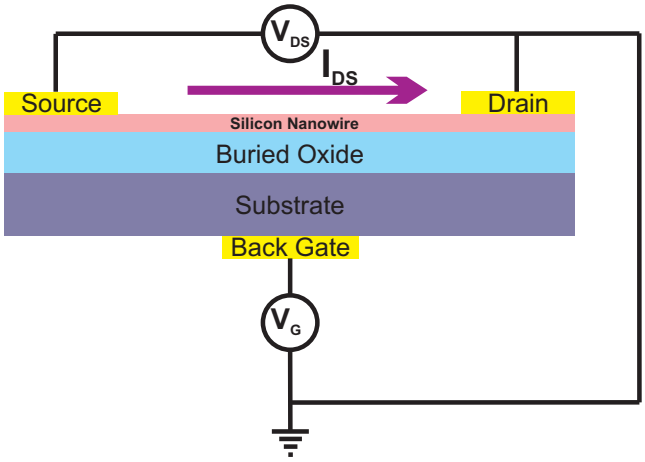


Figure 2.8: Schematic diagram of the electrical setup used for electrical characterization of SiNW Bio-FET

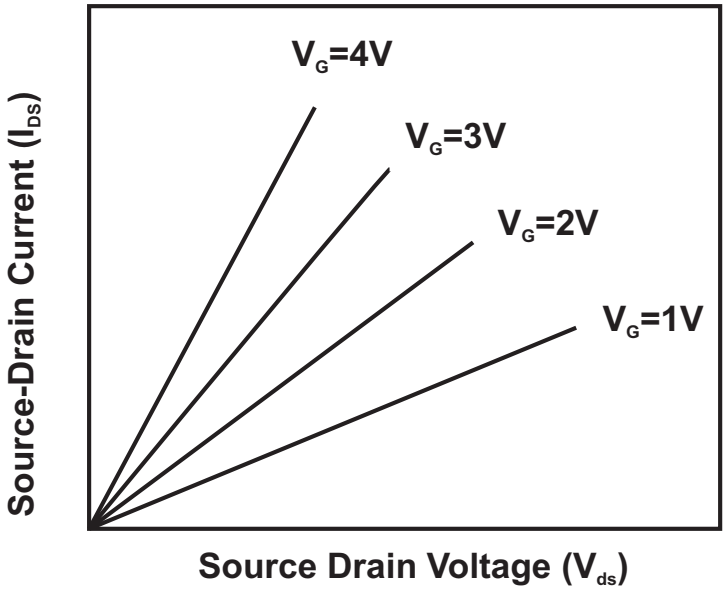


Figure 2.9: Example of I_{DS} vs V_{DS} characteristic of Bio-FET device

And

$$R_{SINW} = \frac{L}{\sigma W t} \tag{2.25}$$

Where σ is the conductivity of SiNW, L is the length of the SiNW, W is the width of the SiNW and t is the thickness of the SiNW. The conductivity can be written as

$$\sigma = q(\mu_p p + \mu_n n) \tag{2.26}$$

Since the p-type has only holes as majority carriers and are responsible for I_{DS}, we can ignore the term μ_n n by considering that $n << p$. Then the conductivity of the SiNW is the sum of doping concentration p_0 and the carriers induced by the gate voltage, p

$$\mu = q\mu_p(p + p_0) \tag{2.27}$$

Putting values in the equation 2.24 gives us

$$I_{DS} = \frac{W\mu_p q(p+p_0)t}{L}V_{DS} \tag{2.28}$$

Expanding the equation makes it

$$I_{DS} = \frac{W\mu_p q(p+p_0)t}{L}V_{DS} \tag{2.29}$$

Expanding the equation makes it

$$I_{DS} = \frac{W\mu_p qpt}{L}V_{DS} + \frac{W\mu_p qp_0t}{L}V_{DS} \tag{2.30}$$

The term $\frac{W\mu_p qp_0t}{L}V_{DS}$ is the constant and can be replaced by K which is the source drain current at 0 V back gate voltage

$$K \equiv \frac{W\mu_p qp_0t}{L}V_{DS} \tag{2.31}$$

Now the total net charge in the SiNW can be written as

$$qpt = \frac{Q}{WL} = \frac{C_{ox}}{WL}V_G = C^*_{ox}V_G \tag{2.32}$$

Where C_{ox} is the capacitance of the buried oxide and C^*_{ox} is the capacitance per unit area. This makes the equation as

$$I_{ds} = \frac{W\mu_p C^*_{ox}}{L}V_G V_{DS} + K \tag{2.33}$$

And

$$C^*_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \tag{2.34}$$

Where $\epsilon_{ox}$is the permittivity of the oxide and t_{ox} is the thickness of the oxide
Since mobility is the measure of how well the holes can move in the SiNW, to get this parameter we have to see the change in source drain current by sweeping the back gate potential. The figure 2.10 shows the behavior of the p-type SiNW by sweeping back gate potential. The slope of this curve can then be expressed as

$$\alpha = \frac{I_{ds}}{V_G} \tag{2.35}$$

By putting the values makes the above equation as

$$\alpha = \frac{W\mu_p C^*_{ox}}{L}V_{DS} \tag{2.36}$$

Replacing C^*_{ox} with $\frac{\epsilon_{ox}}{t_{ox}}$ and isolating μ_p makes the equation as

$$\mu_p = \frac{Lt_{ox}}{W\epsilon_{ox}V_{DS}}\alpha \tag{2.37}$$

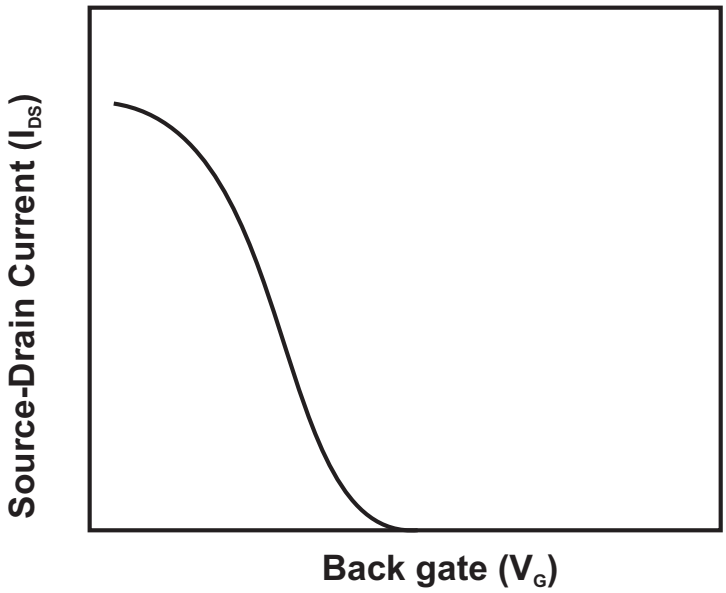


Figure 2.10: The example of source-drain current decrease with the increase in the back gate voltage

2.4.2 Estimation of dopant concentration

The dopant concentration in the SiNW can be estimated by two methods. One is by using Secondary Ion Mass Spectroscopy (SIMS) technique in which high energy ions are bombarded over the silicon surface to extract and count the dopants, and the other is by electrical measurements. By using the equation

$$p_0 = \frac{KL}{W\mu_p qtV_{DS}} \tag{2.38}$$

Different modes of operation in the Bio-FET can be understood well by looking at the Source-Drain Current (I_{DS}) vs back gate voltage curve as shown in figure 2.11.

2.5 Conclusion

Since the aim of the project is to use in-situ doped polysilicon in a junctionless setup, to ensure sensitivity of the SiNW, the role of Debye-screening length and Thomas fermi screening length are considered while developing the fabrication process.

The Debye screening length is dependent on the ionic concentration of the electrolyte in which the biomolecules are present. The lower concentration of ions in the solution makes the Debye screening length higher which results in the increase of detection signal in the sensor caused by the binding of the biomolecules to the oxide surface of SiNW. However, biomolecules are usually present in higher ionic concentration solution, e.g DNA is present in 100 mMol saline solution which results in quite short debye screening length. It is possible to have biomolecules present in diluted buffer solutions, but even so the Debye length is still short, usually not more than 10 nm.

To compensate the effect of short debye screening length, low oxide thickness in the fabrication process is used in this project so that small signals coming from the binding event of biomolecules can be translated into significant change in the

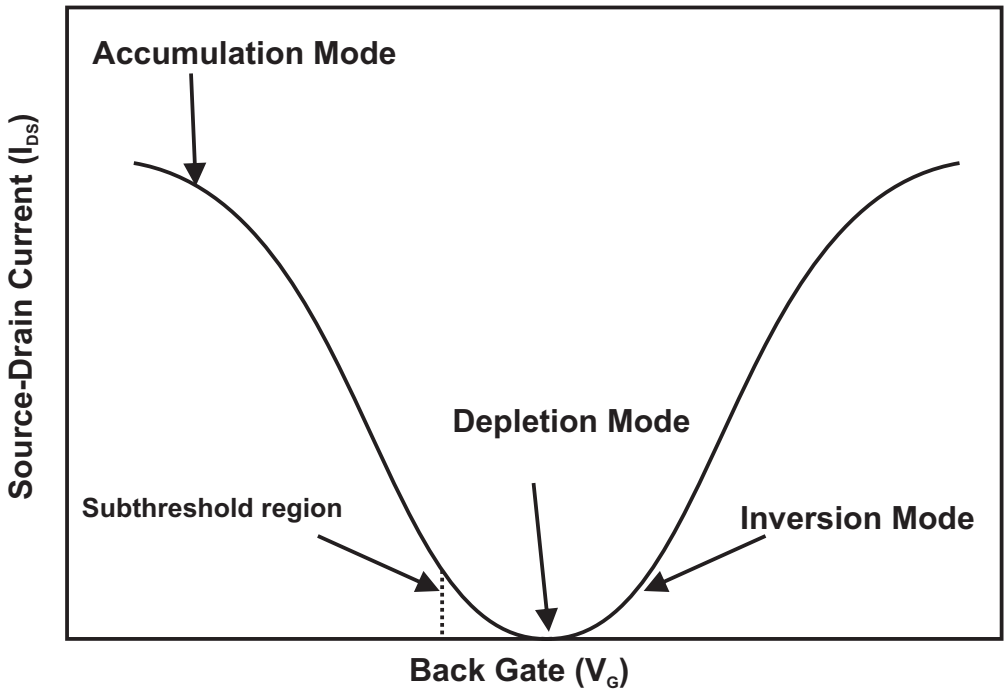


Figure 2.11: An example of different modes of Bio-FET when back gate is swept from negative potential to positive

source-drain current of the SiNW sensor. The dielectric properties of the oxide have been tested by applying liquid gate potential to check any leakages of current from SiNW in to the liquid.

Thomas-Fermi screening length depends on the concentration of the dopants in the SiNW. The low concentration of the dopants gives the high Thomas-fermi screening length which increases the influence of the external charge in the SiNW current flow. This influence can be further enhanced by reducing the dimensions of the SiNW. In the fabrication process development of the in-situ doped polysilicon SiNW the dopant concentration in the SiNW is kept to a low level to ensure the high change in the signal of the SiNW upon binding of the biomolecules to its surface. However, the doping concentration cannot get arbitrarily low, since we also have to ensure a good contact between SiNW and the metal leads. At the same time the dimensions of the SiNW are kept to low level by reducing the thickness and width of the SiNW.

Chapter 3

Fabrication of Devices

This chapter is focused on the novel top-down fabrication technique in which in-situ doped polysilicon is used as the nanowire material. Three processes have been developed during the course of the project; whereby the major difference between those is the patterning method of the silicon nanowire, the metallization technique, and the passivation of the metal electrodes. These processes are termed as 1st generation, 2nd generation and 3rd generation process hereafter.

3.1 Requirements of the device

To develop a process for a FET device, the first step is to list down the requirements of the device for better and accurate sensing. Keeping in view the schematic of the device in figure 3.1, the following are the most important material parameters that need to be considered beforehand:

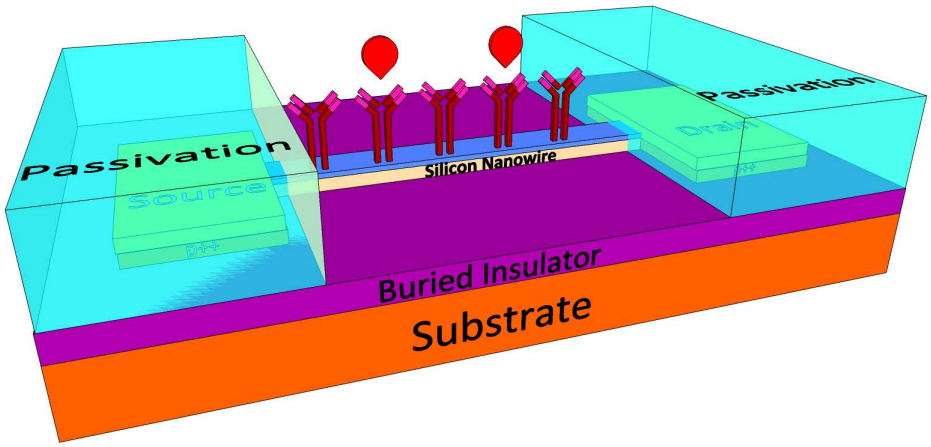


Figure 3.1: Schematic diagram of Bio-FET device with all the required materials

3.1.1 Substrate Selection

Bulk silicon single sided polished wafer, with a resistivity of around Ω-cm, is the most commonly used substrate for FET devices. Its ability to withstand different process conditions like high temperature, reactive chemicals and plasma processes without getting affected makes it suitable for various applications. In this project,

the substrate used in all the generation processes is double side polished <100> p-type silicon with resistivity of around 1-20 Ω-cm and thickness around 350 μm.The main reason to choose less thickness of wafer is to fulfill the requirement of ZIF (Zero Insertion Force) socket which involves the thickness of device to be around 350 μm and to avoid the thinning of the wafer by dry or wet etching process.

3.1.2 Buried Insulator

An insulator is used in the FET device to restrict the current flow within the SiNW and to avoid any leakage of the current into the substrate that may affect the signal. The most common insulator used in FET devices is silicon dioxide (SiO_2), which is normally grown on top of the substrate by a dry or a wet oxidation process at temperatures higher than 1000℃ . This is due to its dielectric properties and its stability at high temperature conditions. The other insulator used in FET devices is stoichiometric silicon nitride (Si_3N_4) which is found to be unstable at high temperatures and exhibits current leakage at high back gate voltages (explained in chapter 6). When the two materials are used together, their combined isolating properties are much better than having any of them alone (explained in chapter 6) [61, 73].

In this project, the first generation process is developed by using SiO_2 as the insulator, the second generation by using only Si_3N_4 as the insulator and the third generation process is developed by stacking SiO_2 and Si_3N_4. The electrical characterization of all the buried insulators is done by applying a back gate potential to check if there is any leakage through the materials after the devices are fabricated.

3.1.3 Silicon Nanowire

The most important component for the Bio-FET device is the SiNW. It's performance as a sensor greatly depends on the material used to make the SiNW. Most of the available studies have been done by using single crystal silicon as the SiNW material [64, 47, 49, 48] and in particular by using the single crystal silicon found on a Silicon-On-Insulator (SOI) wafer. Due to the high cost of SOI wafers, polysilicon has also been studied in the Bio-FET setup as a low cost alternative and has demonstrated promising results [73, 58, 74].In this project a novel material, in-situ doped polysilicon, with boron as the dopant in a junction-less setup has been studied as a robust, low cost alternative to the aforementioned materials. Furthermore, different thicknesses of this material were tested to determine the optimal detection limits.

3.1.4 Source-Drain Doping

To enable the flow of current from source to drain when applying a potential across the SiNW, metal contacts are made on top of the polysilicon source and drain to avoid problems mentioned in chapter 8. To avoid Schottky-barriers between metal-silicon contacts, the source and drain are usually highly doped e.g. by an ion-implantation method [61, 64, 47, 58, 74, 75, 51, 55] [56, 76, 77, 60] or, alternatively, SOI wafers with resistivity of device layer around 10-40 Ω-cm are used [49, 48].

In this project, we investigate the use of in-situ boron doped polysilicon with the lowest possible dopant concentration that can avoid Schottkey-barrier between metal-silicon contacts and as well as provide optimum sensitivity in the fabricated

SiNWs biosensors. Three different recipes were made in the furnace with varying diborane (B_2H_6) gas flow i.e. 3 sccm, 5 sccm and 7 sccm respectively while keeping the silane (SiH_4) gas flow to a constant number that are used for deposition of in-situ doped polysilicon. The SiNWs were fabricated by these recipes using first generation process explained in section 3.3 and were tested by applying Alternative Current (AC) by using the measurement setup explained in section 5.1. For the first two recipes with B_2H_6 gas flow of 3 and 5 sccm, the Schottkey-barrier was observed between metal-silicon, where a phase shift of more than 30 degrees was observed in the AC measurements. No phase shift was observed in the last recipe with B_2H_6 flow of 7 sccm.

This recipe is investigated as a next step by making Secondary Ion Mass Spectroscopy (SIMS) measurements on the polysilicon samples for the estimation of boron dopant concentration. The dopant concentration was found to be around $3 \times 10^{18} - 5 \times 10^{18}$ atoms/cm^3 that can provide both a reliable metal-silicon contact and an acceptable FET behavior. The metal-silicon contact is further improved by an annealing step after metal deposition.

3.1.5 Patterning of Silicon Nanowire

Several techniques have been adopted to pattern SiNW that have their lateral dimension in nanometers. These techniques can broadly be categorized into dry etching and wet etching i.e. a plasma based etch process for dry etching and liquid phase etching for wet etch. Most of them rely on expensive techniques, like use of e-beam lithography or Nano imprinting in order to create the SiNW pattern on a mask material, usually SiO_2. In few cases optical lithography is used for low cost production. The patterned mask structure is then used for wet etch in tetra-methyl-ammonium-hydroxide (TMAH) to pattern SiNW [64, 47, 48, 56, 76, 77, 78]. In some cases, dry etching is also used to pattern the SiNW [49, 58, 60].

In this project, the 1st generation process was developed by using dry etching to pattern SiNW, whereas a wet etching method was adopted in the 2nd and 3rd generation process.

3.1.6 Metallization of Source-Drain

To interface the SiNW with the electrical read out systems, metallization of the source and the drain is required. As discussed above, the important factor is the barrier height between metal and silicon. In this project, the metal chosen for the device is gold (Au) not only due to its resistivity against oxidation and corrosion but also due to the fact that its barrier height is around 0.87 eV for a p-type silicon, which can give a better contact if the doping concentration in silicon is around 1×10^{18} [79, 80]. However, adhesion of Au to silicon (Si) is not good and to improve the adhesion Chromium (Cr) is used as an adhesion layer for the first generation process and a Titanium-Tungsten (TiW) alloy is used as an adhesion and metal diffusion barrier layer for the 3rd generation process.

Since annealing of the contacts in a forming gas like N_2 at around 300℃-550℃ improves the contact, in this project the contacts are annealed at 300℃ in 1st generation whereas 350℃ for 1 hour in 2nd and 3rd generation.

3.1.7 Passivation

Since the SiNW will be used for biological sample detection and it will be exposed to liquid, the passivation of the electrical contacts is deemed necessary to avoid any short circuits, noise and damage to the device. For this purpose, materials with high dielectric strength and low temperature deposition are needed. The most commonly used dielectric materials are Plasma Enhanced Chemical Vapor Deposition (PECVD) Si_3N_4 [60, 81, 45, 63] or a stack of PECVD SiO_2 and Si_3N_4 [64, 47, 55]. Use of polymers like SU8, epoxy, parylene and PDMS as the passivation layer [49, 48, 51, 56, 60] that also acts like a microfluidic channel on top of SiNW, has also been demonstrated.

In this project two polymer materials have been tested, i.e. SU8 and Polyimide. Sputtered Si_3N_4 has also been tested as a passivation layer. Due to the large amount of Au on the wafer surface, around 15%, it was not possible to use the customary PECVD Si_3N_4, due to cleanroom restrictions.

3.2 Design of the sensor

As four inch wafers are to be used in the fabrication process, the chip containing the FET sensors have been assigned the dimensions of $15.2cm \times 5.5cm$, which makes us able to fit around 54 chips on one wafer. The shape of the chips is such that they fit in a ten pin Zero-Insertion-Force (ZIF) socket that provides a better interface connection of the chip to the electrical read-out system. This can be a computer with a LabVIEW measurement program or a CMOS based read-out system (these systems are discussed in chapter 5). To interface the chip with the ZIF socket, the ten contact pads are designed so that eight of them are assigned to the source and drain of four nanowires while two contact pads are left for the side gates that can be used to gate the SiNW. This design was made in the NaBIS research group by former master student Michael Jørgensen. The purpose of the side gate was to control the current flow in the SiNW by applying potential from the side as well. The side gate electrodes were later removed in this project during characterization of SiNW as is discussed in details in chapter 6. Figure 3.2 below shows an L-edit image of one of the sensors in the wafer.

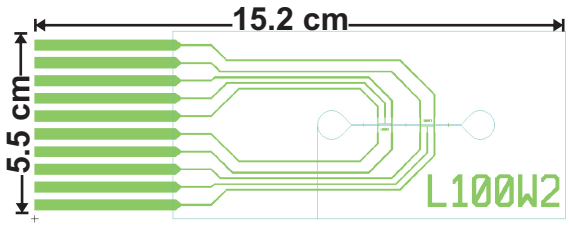


Figure 3.2: An Image from the L-edit design of the sensor showing all the three layers of the sensor

The whole wafer is divided into four types of chips which are different from each other in terms of dimensions of the SiNW. These types along with their dimensions are shown in table 3.1

The main reason to choose 2μm width was to remain in the limitations of optical lithography technique to pattern SiNW. Though it is possible to go down in the

Dimensions	Chip Type 1	Chip Type 2	Chip Type 3	Chip type 4
$Length \times Width$ (μm)	70×2	120×2	70×5	120×5

Table 3.1: Types of chips in the wafer level design

width by using photoresist with less thickness or by using deep UV lithography, but the aim for this project was to use standardized techniques that do not require any specialized mask design (as required for deep UV lithography), or more expensive mask production. The minimum linewidth at Danchip cleanroom using standard UV lithography and the conventional mask production is 1.7μm . The 5μm width was decided to check if the change in the width of the SiNW also affects the sensitivity of the SiNW. The 70μm length was chosen to do the sensing in the flow of cells which are several microns in size. The 120μm length was decided to check the influence of length on the behavior of the SiNW sensitivity. These considerations were made during the Master project by Michael Jørgensen.

Other than the four SiNW wires that have source and drain connected to the bonding pads, four SiNW are also included in the chip for fluorescence detection experiments. Each chip in the wafer has a unique name which is based on the location of the chip in the wafer. The whole wafer is divided into four big columns, which are named as B, C, D and E, and two small columns, namely 0 and F, as they are located into two extreme positions of the wafer and cannot contain many chips. Another label that can be found on the chip is the dimensions of the SiNW when it is not connected with the source and drain. Figure 3.3 shows a zoomed-in image with all the components of the sensor.

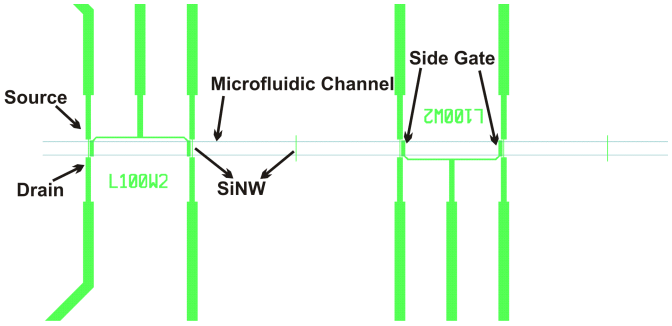


Figure 3.3: Components of the sensor (zoomed in image showing source, drain, SiNW, microfluidic channel, side gate and length and width of the SiNW for florescence detection)

The sensor contains three mask layers: the SiNW, the metal electrodes and the microfluidic channel/ passivation layer.

3.3 First Generation Fabrication Process

In this section, the fabrication steps for the first generation process are explained in detail.

3.3.1 Buried Insulator

A p-type <100> double side polished bulk silicon wafer of thickness around 350μm with resistivity of around 1-20 Ω-cm is used as the substrate for the SiNW Bio-FET. As a first step, the dry oxidation is performed at 1100℃ to get 170 nm of SiO_2 as a buried layer. Figure 3.4 shows the schematic of device after step 1.

Figure 3.4: Schematic view after the first step of the process

3.3.2 In-situ Doped Polysilicon Deposition

The wafer is then transported to the Low Pressure Chemical Deposition (LPCVD) furnace for deposition of 50 nm of polysilicon at around 620℃. The gas flows of diborane (B_2H_6) and silane (SiH_4) are adjusted in the ratio so that the boron dopant concentration should be around $3 \times 10^{18} - 5 \times 10^{18}$ atoms/cm^3. The detailed recipe used with all the parameters can be found in the appendix. Since both the furnaces i.e. oxidation and polysilicon, deposit oxide and polysilicon on both sides, these layers can be removed from the bottom of the wafer by a wet etch process, first in a mixture of nitric Acid (HNO_3), buffered Hydro fluoric acid (BHF) and water (H_2O) at a ratio of 20 : 1 : 20 for polysilicon etch, and then in BHF alone to remove (SiO_2). The front side of the wafer is protected by applying the nitro tape, also known as blue tape. Figure 3.5 below shows the schematic of device after step 2.

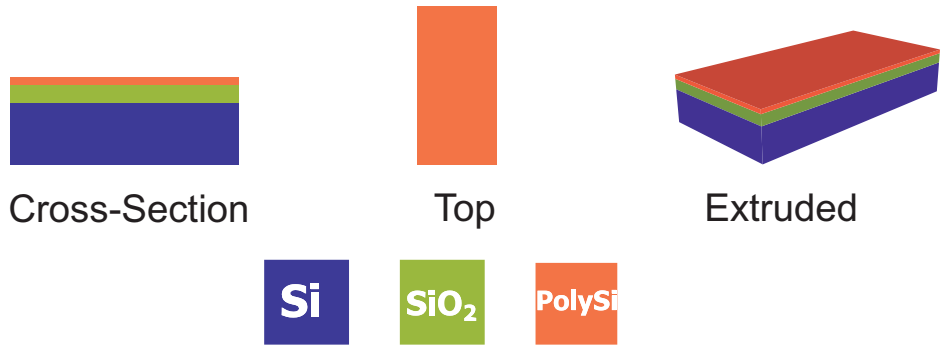


Figure 3.5: Schematic view after the 2nd step of the process

3.3.3 Patterning of Silicon Nanowire

As a third step, the patterning of the SiNW is done by first spinning a photoresist layer and then doing optical lithography followed by reactive ion etching (RIE) in the

presence of sulfur hexaflouride (SF_6) and Oxygen (O_2) for approximately 25 seconds by using the end point detection system in the machine to avoid any damage to the buried oxide [82, 83, 84]. The detailed recipe is available in the appendix. The photoresist is removed afterwards. Figure 3.6 shows the schematic of the device after step 3.

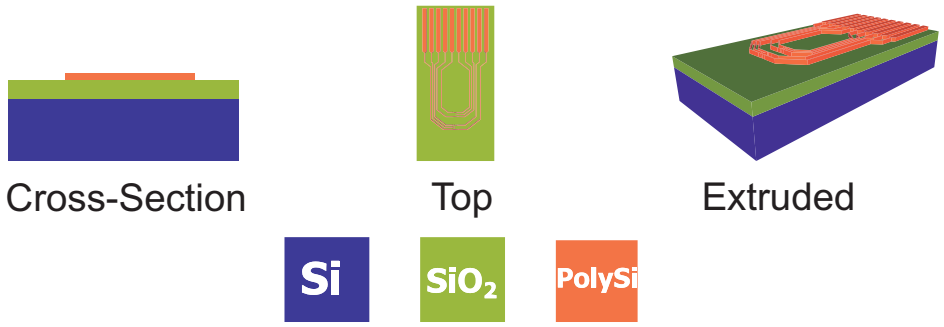


Figure 3.6: Schematic view after the 3rd step of the process

3.3.4 Metallization of Source and Drain

After the patterning of SiNW, electrodes are formed over the source and drain by optical lithography and a lift-off process. 20 nm chromium (Cr) and 100 nm gold (Au) are deposited by e-beam evaporation. The pattern of electrodes is achieved by ultra-sonication in acetone bath for 10 minutes. Figure 3.7 shows the schematic after this process step.

Figure 3.7: Schematic view after the 4th step of the process

3.3.5 Passivation

The electrodes need to be passivated afterwards. In this generation of the process, initial batches were produced using SU-8 polymer, but due to problems in bio sensing discussed in chapter 7 it was replaced by polyimide which is used as passivation layer due to its better dielectric properties [85, 86] and ability to be used as microfluidic channel that will help in better execution of bio sensing experiments. The curing conditions of polyimide are 350℃ for 1 hour which also anneals the electrodes for better ohmic contact. A detailed fabrication process for the formation of polyimide

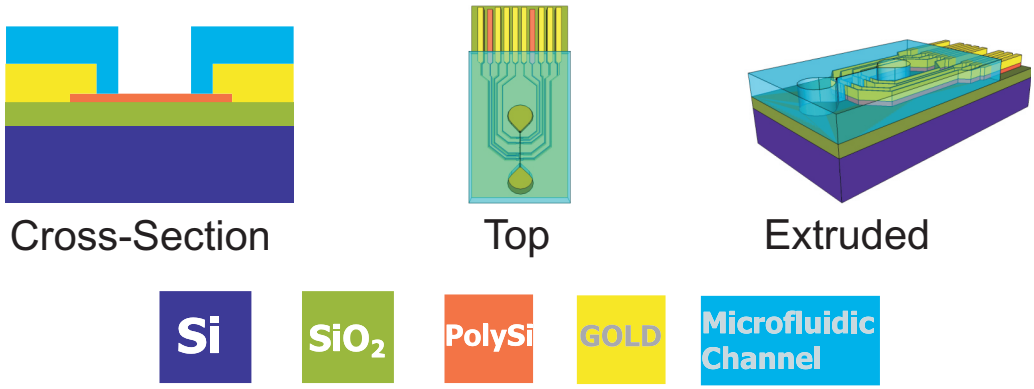


Figure 3.8: Schematic view after the 5th step of the process

microfluidic channels on top of SiNW is explained in chapter 4. Figure 3.8 below shows the schematic after the fifth process step.

After the fabrication process, the chips are diced and tested in the electrical measurement setup. The details of the electrical characterization are discussed in Chapter 6. Images of the finished chips are shown in figure 3.9.

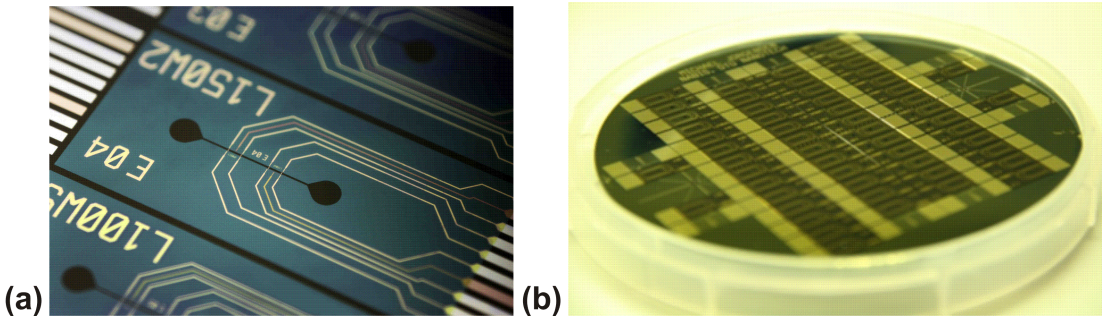


Figure 3.9: (a) Close-up image of a chip after fabrication with PI microfluidic channel (b) Image of a full wafer after fabrication with SU-8 microfluidic channel

3.4 Second Generation Fabrication Process

Based on the bio sensing results explained in chapter 7 and the electrical characterization results of the first generation process explained in chapter 6, improvements were made in the fabrication process that led to the development of the second generation process. The main changes in the process are listed below:

- Change in the grain size of the polysilicon after deposition by an annealing step in order to improve the conductivity of the SiNW.
- Reduction in the thickness and width of the SiNW in order to have smaller and fewer grain boundaries, which will help in achieving depletion mode at smaller back gate potentials.
- Reduction in the thickness of the buried insulator in order to achieve a stronger influence of the electric field on the I_{DS} of the SiNW.

- Replace the SiO_2 layer with Si_3N_4 to only functionalize the top oxide of SiNW and not the whole buried insulator, since the functionalization protocol using silanization method (explained in chapter 7) will attach the biomarkers to SiO_2.

- Reduction in the width of the SiNW while keeping the same masks (widths of 2 and 5μm) by replacing the dry etch with a wet etch method for patterning SiNW. In this way, the effect of plasma etching on the insulator's dielectric strength will also be nullified.

The process steps that are changed from the 1st generation process are explained below.

3.4.1 Replacement of Buried Insulator

As a first step, the 170 nm thick buried oxide was replaced by 54 nm thick stoichiometric Si_3N_4 grown by an LPCVD process at around and to reduce the thickness of the buried insulator, a stack of 30 nm dry oxide is grown at around 800℃ and the dielectric strength of the layer was measured using the setup explained in chapter 5. The dielectric strength of the Si_3N_4 was found to be in the same range as that of SiO_2 i.e. 1 V/nm.

3.4.2 Polysilicon Deposition

The thickness of the polysilicon was reduced from 50 nm to 30 nm as a second step by reducing the deposition time from 5 minutes 45 seconds to 3 minutes 30 seconds.

3.4.3 Annealing

Thirdly, to change the grain size of the polysilicon aiming to improve the conductivity of the SiNW, wafers were annealed at 900℃ for 30 mins soon after polysilicon deposition. An average grain size was measured to be around 25 nm by using Scanning Electron Microscopy (SEM). Figure 3.10 shows the SEM image of an edge of SiNW with the measurements made for the grain size of the polysilicon after patterning the SiNW.

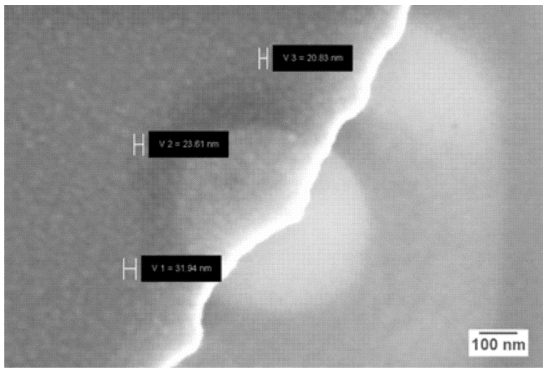


Figure 3.10: SEM Image of the grain size of 30 nm thick polysilicon after patterning of SiNW

3.4.4 Patterning of SiNW

To reduce the width of the SiNW while keeping the same mask specification, the wet etching method is adopted to pattern them. As a first step, low stress PECVD Si_3N_4 of around 220 nm thickness is deposited on top of polysilicon followed by patterning of the nitride by dry etching in the mixture of Octa-fluoro-cyclo-butane (C_4F_8) and Helium (He) gas. Before removing the photoresist mask, the width of the nitride layer is reduced to around 800 nm by dipping the wafer in BHF with wetting agent (also known as IMEC clean) for 5 minutes. This mask is then used for potassium hydroxide (KOH) etching at 25℃ to pattern polysilicon. Figure 3.11 shows the schematic diagram of the fabrication steps for 2nd generation process.

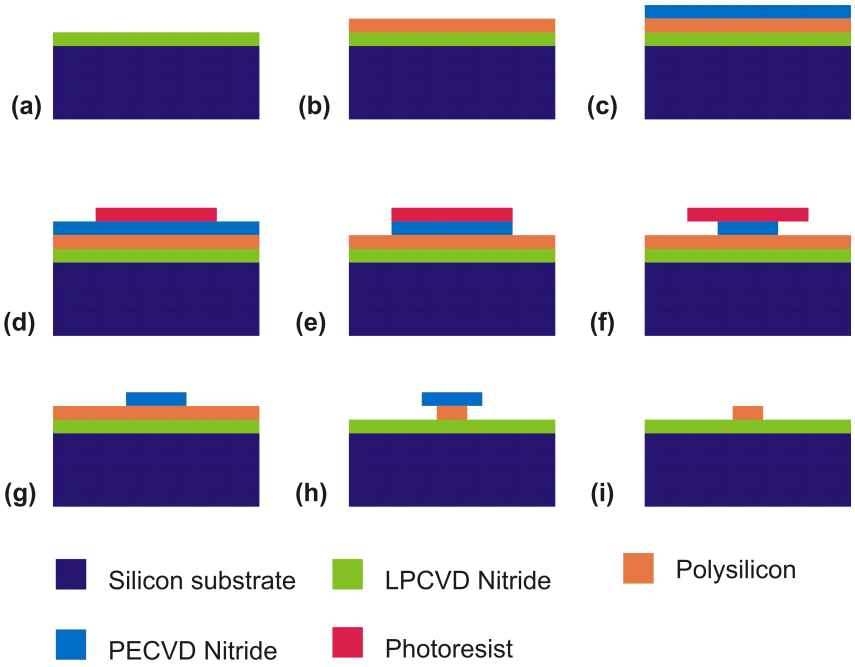


Figure 3.11: Schematic of all the steps involved in patterning of SiNW by wet etching in 2nd generation process

By the under etching method, SiNW with dimensions down to approximately 300 nm width are achieved. Figure 3.12 shows a SEM image of the SiNW after patterning. It can be seen that the rough edges of the SiNW are due to variable etching rate across different grains of polysilicon.

3.4.5 Passivation

At the same time, during the electrical measurements it was found that in some contacts there was a cross-connection which could be due to bad passivation of PI. By following the supplier's manual it was found that annealing at 350℃ improves the passivation properties of PI.

3.5 Third Generation Fabrication Process

The sensing results of NKG2D cancer biomarker discussed in chapter 7 didn't show significant change in the signal of SiNW upon binding of analyte to it. Moreover,

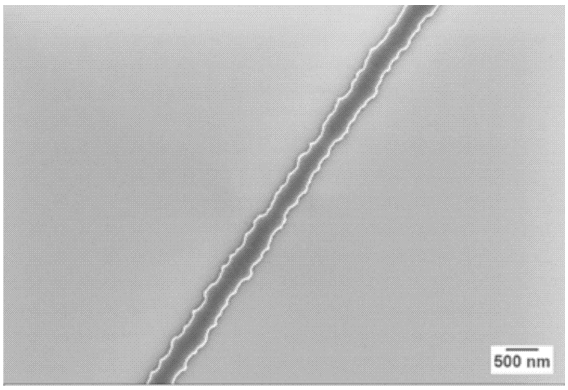


Figure 3.12: SEM Image of the 280 nm wide SiNW annealed at 900℃ for 30 mins after wet etching

electrical characterization of the 2nd generation process showed that the full depletion of the SiNW was still not achieved even by going high in back gate voltage of up to 15 V. It was not possible to go further high as the leakage current from the substrate would start to pass through the buried nitride layer and dominate the signals acquired through the SiNW. The high leakage current at such a low potential was found to be due to the fact that at high temperatures the difference in the thermal expansion of bulk silicon substrate and Si_3N_4 results in the dislocations of the grains at Si/Si_3N_4 interface layer which results in crack initiation and results in weak insulation properties of the nitride layer [87]. In addition to that, the passivation properties of PI were not good by curing it at 300℃ for 1 hour.

To overcome the problems mentioned above and to improve the device performance, following steps were taken in the 3rd generation process.

3.5.1 Oxidation and Annealing

After polysilicon deposition dry oxidation for 1 min at 1100℃ followed by annealing for 20 min at 1100℃ should change the grain size and improve the conductivity of the SiNW. This hypothesis was inspired by the findings of [88, 89, 90]

After this process the thickness of the SiNW is reduced down to 20 nm. Figure 3.13 shows the SEM images taken after patterning of the SiNW, which shows less roughness at the edges of the SiNW possibly due to bigger grain size in polysilicon.

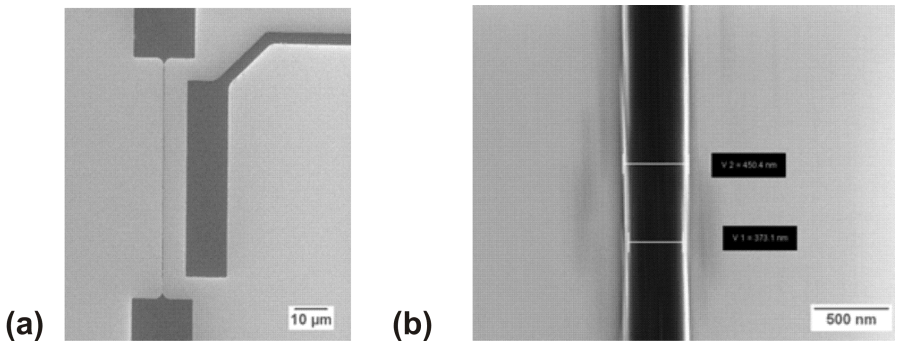


Figure 3.13: SEM Image of the 370 nm wide SiNW oxidized for 1 min and annealed for 30 mins at 1100℃(a) Image with source-drain and SiNW (b) zoomed in image of the SiNW

3.5.2 Addition of Dry oxide in buried insulator

To reduce the effect of the dislocation, 30 nm thick dry oxide grown at 1100℃ was added between the bulk silicon and the Si_3N_4 layer, which resulted in the good insulation properties of the combined insulators (explained in chapter 6)

3.5.3 Metallization Replacement

It was also observed that during fabrication, when the wafer is annealed at 350℃ for curing PI to improve passivation, some of the devices stopped working due to loss of source-drain connection. The reason was found to be that Au diffuses through Cr at high temperatures [91, 92] and forms silicide with very thin polysilicon, which causes discontinuity in the source-drain connection in some of the devices in the whole wafer. The metallization layers for the electrodes were then replaced by 200 nm magnetron sputtered TiW followed by e-beam deposition of 150 nm Au. Radio frequency (RF) cleaning is also done for half an hour before sputtering TiW for better adhesion and improved contact. The TiW not only acts like an adhesion layer but also as a diffusion barrier layer for Au to make eutectic contact with thin polysilicon when it is annealed at high temperature for improving contact resistance.

3.5.4 Passivation of Electrodes

To improve the passivation of PI it was cured at 350℃ for 1 hr. After applying the changes in the metallization step of fabrication process and reducing the thickness of the SiNW it was found that the SiNWs had lost the electrical connection from source-drain, during the the electrical characterization experiments. To troubleshoot this, two probe measurements were made after each fabrication step. It was found that the SiNW break down happens when the PI microfluidic channels are formed over the SiNWs. This problem was only found on the SiNWs that were oxidized and annealed. The reason for this breakage was later found to be that the SiNWs got so thin and delicate that they could not bear the stresses that arise from the curing process of PI. This problem was solved when PI was replaced by sputtered Si_3N_4 as the passivation layer which is patterned through a lift-off process. The process parameters used for sputtered Si_3N_4 are attached in the appendix.

3.5.5 Results

Figure 3.14 shows the images after fabrication of SiNW by 3rd generation process.

The electrical characterization of the devices fabricated by using 3rd generation process shows significant improvement in the performance of the SiNW. To check the variation in width of the SiNW over the whole wafer after wet etch process, width measurements were done on the chips at the edges and center of the wafer. Figure 3.15 shows the range of the achieved SiNW widths across the wafer.

It is observed that the SiNW in the center of the wafer were etched slow compared to the SiNW on the edges. It can relate to the non-uniformity in the plasma etching of the Si_3N_4 mask followed by wet etch in BHF. The other possible reason could be the temperature gradient inside the KOH wet etch bath which etches the SiNW at the edges faster compared to the SiNW at the center.

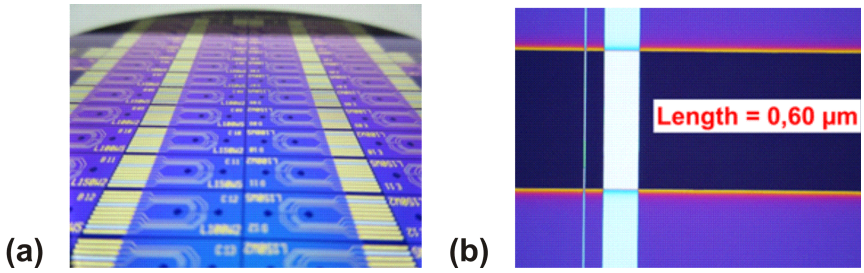


Figure 3.14: Images after fabrication by 3rd generation process (a) Wafer before dicing (b) SiNW with side gate and sputtered Si_3N_4 passivation observed under optical microscope

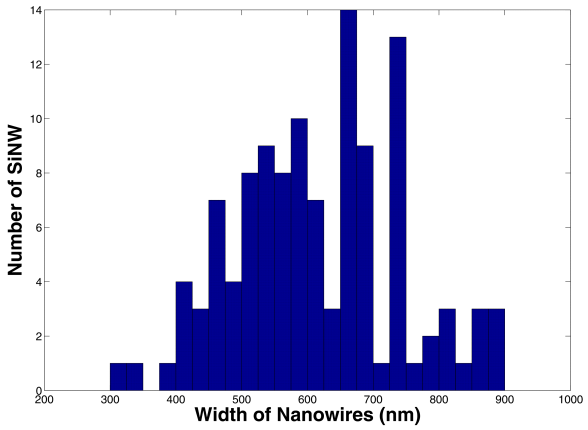


Figure 3.15: Histogram of the width measurements of SiNW made on all chips with 2μm width in mask

Chapter 4

Fabrication of Microfluidic Channel

In this chapter, a novel fabrication technique for developing microfluidic channels on biosensor devices by using polyimide (PI) as fabrication material is explained in detail. The first section sheds light over the advantages of using PI as fabrication material for biosensors over other commonly used polymers. Thereafter, the fabrication process of making microfluidic channel in PI is elaborated in detail by using two different masking materials for patterning it by a dry etch process. It is then compared to the most commonly used epoxy polymer SU-8 in terms of simplified and robust fabrication process with better uniformity on wafer level.

Closed-Channel microfluidics is also demonstrated in this chapter by wafer level bonding of partially cured (not fully imidized) PI to PI and to glass followed by dicing of devices and bond strength tests. The first test is done by hydrodynamic focusing of red fluid with blue fluid in a microfluidic channel formed by bonding PI to PI. Pressure drop measurements are also done as a second test to check the deformation of the microfluidic channel at high pressures.

Lastly, laser micromachining and milling techniques, used to make the holes in the glass wafer to form inlets and outlets for fluid flow in the microfluidic channels, are discussed.

4.1 Advantages of polyimide

The invention of inkjet printers was one of the first demonstrations of microfluidic based devices that was commercialized for mass production. Since then microfluidic systems have made their way into medical diagnostic devices, chemistry and biotechnology. The main advantage of microfluidic systems is the low volume of fluid that can be used for analysis of different systems, which has led to the concept of lab-on-a-chip and µTAS (Micro Total Analysis Systems)[93] but as the system goes down to micrometer scale, the fluid pressure gets higher and requires strong material that can sustain such pressure levels. The most commonly used polymers for microfluidics systems accomplishing this requirement are Poly-di-methyl-siloxane (PDMS), Poly-methyl meth-acrylate (PMMA) and SU-8.

Recent development in the medical diagnostics field, especially Point-Of-Care (POC) devices, has increased the demand of multifunctional materials that can be used to fabricate complex systems with diverse functions, compact size and integration of microelectronics read-out systems. The above mentioned materials for microfluidics systems have limitations in their physicochemical properties and can-

not fulfill all the requirements of the modern POC devices [86]. For example PDMS and PMMA are not stable against many chemicals that are used in microelectronics device fabrication processes [94, 95] which imposes constraints in integrating microfluidics with microelectronics systems. Similarly SU-8 epoxy resin, with a complex fabrication process, is very sensitive to the processing conditions and requires a lot of parameters optimization like soft baking, UV exposure, post exposure, development and final baking step. If the conditions are slightly changed during the processing, they can cause cracks, delamination or bad resolution of the channels [96].

PI has recently emerged as a strong candidate for building the microfluidic systems [93, 97, 98, 99, 100] due to its high resistance against many harsh chemicals, stability at high temperatures, high dielectric strength, and biocompatibility along with the simple fabrication process. In this project, material properties of non-photosensitive PI are explored and PI is implemented as a passivation layer and microfluidic channel on a SiNW Bio-FET device. The main strength of choosing PI for the Bio-FET device is its proven resistance against all the organic solvents as well as very low etch rates in strong acids like BHF that are used in the fabrication process of SiNW [101]. Moreover, a glass transition temperature of around 325℃ and dielectric constant of around 3.4 (at 1kHz and room temperature) [85] makes it a strong contender to be used as passivation layer for SiNW Bio-FET sensor.

4.2 Fabrication Process of Microfluidic Channels

PI-2574, supplied by HD $Microsystems^{TM}$, is selected for the fabrication process due to its self-priming ability that will enable us to achieve various thicknesses for the microfluidic channel by multi-coating. The fabrication process is developed and optimized by using a quartz substrate as a first step and then it is used to fabricate microfluidic channels on SiNW Bio-FET devices. Two fabrication techniques are developed, one by using PECVD Si_3N_4 as a masking material to pattern PI by dry etching and the other by using Al mask. Both the techniques are explained below.

4.2.1 Fabrication using PECVD Si_3N_4 mask

This fabrication process consists of six major steps:

- Spin coating of 10μm PI over 4 inch quartz wafer at 2400 rpm for 30 seconds with 100 rpm/s ramp rate. Soft baking is done for 5 minutes at 120℃ followed by partial curing for 1 hour at 300℃.
- Deposition of 120 nm of PECVD Si_3N_4 mask at 300℃ (the detailed recipe can be found in Appendix)
- Spin coating and patterning 1.5μm photoresist by photolithography
- Dry etching of PECVD Si_3N_4 and removing photoresist in acetone
- Dry etching of PI
- Removing Si_3N_4 mask by wet etching in BHF

A schematic diagram of the fabrication process is shown in figure 4.1.

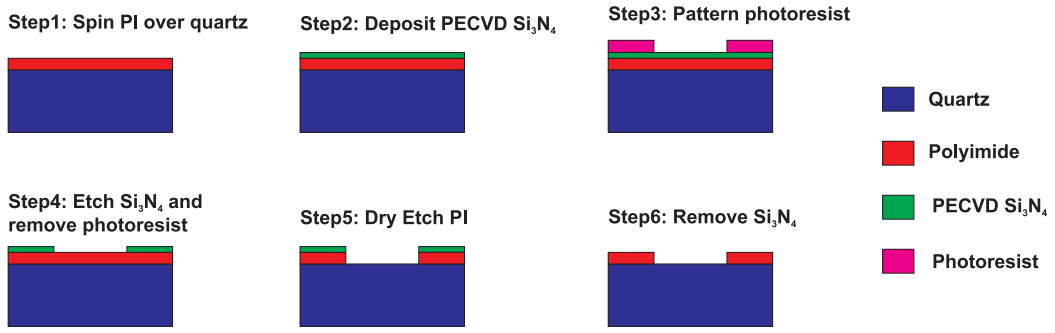


Figure 4.1: Schematic diagram of step by step fabrication process of microfluidic channel using PECVD Si_3N_4 mask

4.2.2 Fabrication using Al mask

The fabrication steps for this process are as follows:

- Spin coating of PI with the same parameters as for Si_3N_4 mask. For thicknesses $> 10\mu$m, the coating and soft baking steps are repeated and the final baking is done at 250℃ for 1 hr to partially cure the PI.
- Spin coating and patterning of photoresist by photolithography followed by 3 minutes descumming in plasma asher to improve the adhesion of Al on PI surface
- Deposition of 100 nm of Al by e-beam evaporation
- Lift-off of Al in acetone with ultrasonic to get the pattern of Al mask
- Dry etching of PI
- Removing Al mask in MF-322 developer solution

The schematic diagram in figure 4.2 shows all the fabrication steps

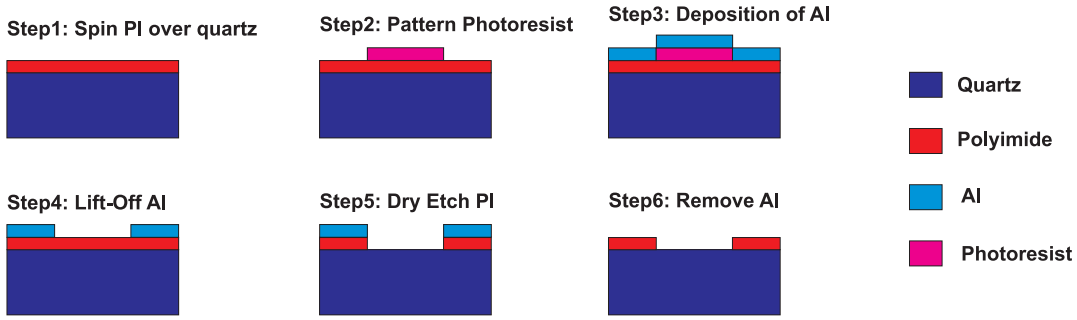


Figure 4.2: Schematic diagram of step by step fabrication process of microfluidic channel using Al mask

4.3 Optimization of parameters for dry etching of PI

Two etching systems, the Reactive Ion Etcher (RIE) and the Inductively Coupled Plasma (ICP) etcher, which are based on parallel plate reactor and inductively coupled barrel respectively [102], are used to develop and optimize the etching recipe for PI. The starting parameters were taken from the previous work done in [98, 100, 102]. For Si_3N_4 mask the dry etch of PI is done in the presence of O_2 and Ar mixture whereas for Al mask O_2 and CF_4/SF_6 mixture is used to etch PI. The main reason to avoid fluorine based gases for Si_3N_4 mask is that they attack the mask and cannot be used for long (> 5 min) etching times.

In plasma etch systems, the etching rate and profile is mainly controlled by pressure, power applied for plasma generation and ratio of gas flows in the chamber since they control the number of reactive ions and their bombardment energy that are responsible for etching the target layer [102]. Keeping in mind the goal of reaching high etch rates, the optimization of the above mentioned parameters in both RIE and ICP systems are explained below:

4.3.1 Parameters with Si_3N_4 mask

For Si3N4 mask, the highest etch rate in RIE was achieved by using the mixture of 98% O_2 and 2% Ar, 200 mTorr as pressure and 100 W applied power while for ICP the highest etch rate was achieved by using 98% O_2 and 2% Ar mixture, 80 m Torr as pressure and 150 W applied power. The etch rate increases by changing power applied for both systems and depicted in figure 4.3.

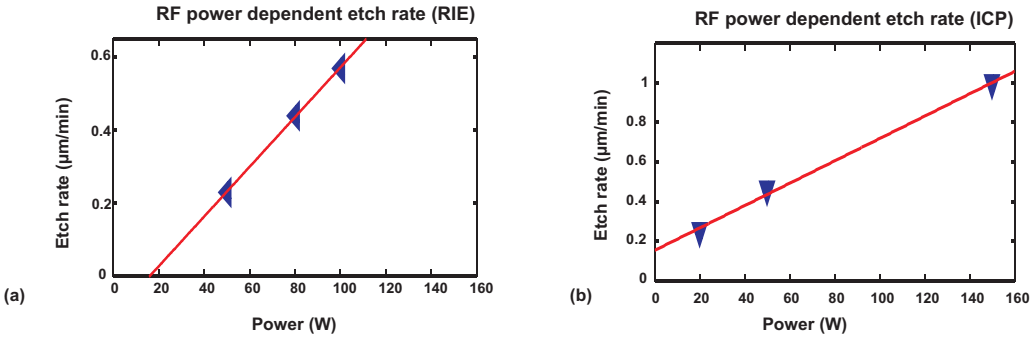


Figure 4.3: Etch rate of partially cured PI as a function of power applied in the chamber with Si_3N_4 mask (a) In RIE the pressure is 200 mTorr and the ratio of O_2/Ar is 98/2 (b) In ICP the pressure is 80 mTorr, the ratio of O_2/Ar is 98/2 and coil power is 2000 W

After etching, grass-like residues were observed at the bottom of the microfluidic channel and after investigation, it was found to be due to the presence of the silane based primer that is mixed in the PI, which does not get etched and settles down at the bottom. To remove these residues, the last 1μm of the microfluidic channel was etched in O_2 and CF_4 mixture in the ratio 80/20. The figure 4.4 shows the SEM images of grass-like residues and the residue free surface after this treatment.

The etch rate could not be raised further because higher power results in the

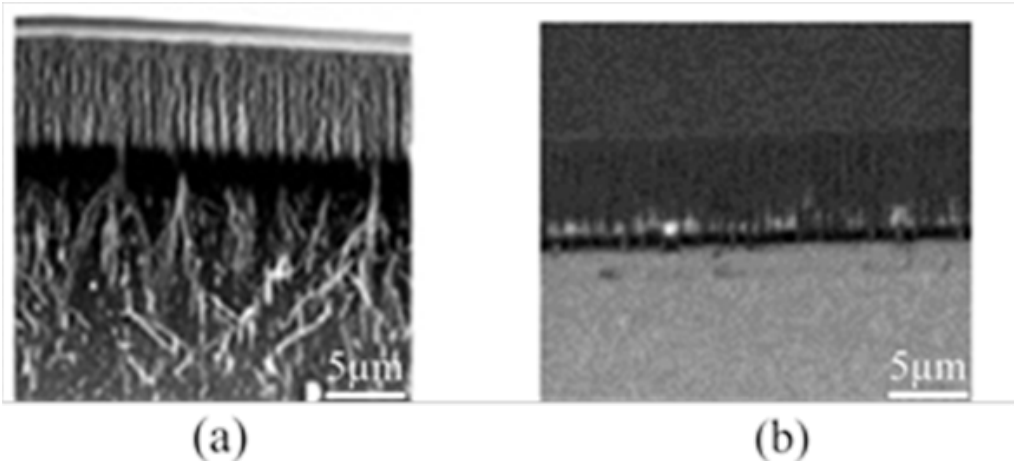


Figure 4.4: SEM images after etching of partially cured PI using Si_3N_4 mask in RIE (a) Residues are visible if CF_4 is not used at all for etching PI (b) No residues are visible if the last 1μm of PI is etched with mixture of O_2 and CF_4

over-heating of the substrate and causes the residues to burn, which makes them difficult to remove later.

4.3.2 Parameters with Al mask

Fluorine based gas was included as a next step in the optimization of the etching recipe to get a residue free surface and the Si_3N_4 mask was replaced by Al mask to get the microfluidic channel's height to be bigger than 10μm.

In ICP, a O_2/SF_6 gas mixture (80:20) was used to etch PI and in RIE the gas mixture was O_2/CF_4 in a ratio of 94:6. The etch rate was first characterized by changing the applied power in both the systems while keeping the other parameters constant. Figure 4.5 shows the etch rate increase by increasing power in both systems.

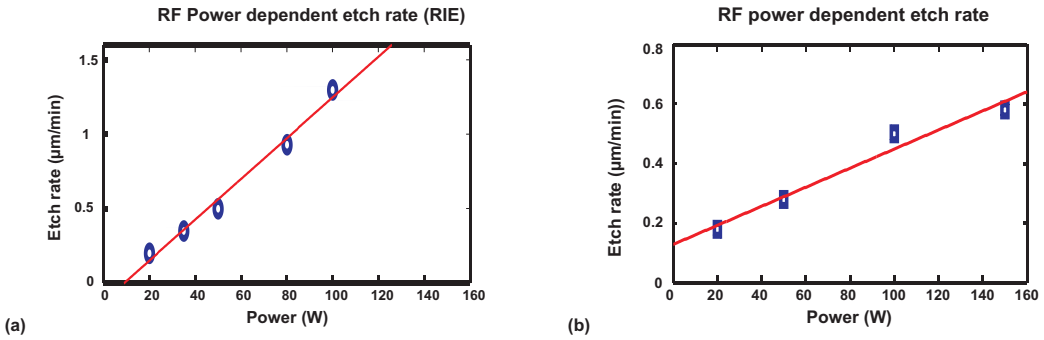


Figure 4.5: Etch rate of partially cured PI as function of power using Al mask (a) The pressure in the chamber is 200 mTorr and the ratio of O_2/CF_4 is 94/6 in RIE (b) The pressure in the chamber is 50 mTorr and the ratio of O_2/SF_6 is 80/20 with coil power of 2000 W in ICP

As a second characterization step, the pressure in the chamber was changed while the power and gas flow ratio were kept constant. In RIE the power applied was set to 20 W and the ratio of O_2/CFO_4 was 85/15 whereas, in ICP the power applied

was 200 W, the ratio of O_2/SF_6 was 80/20 and the coil power was 2000 W. Figure 4.6 shows the etch rate characterization on both the systems.

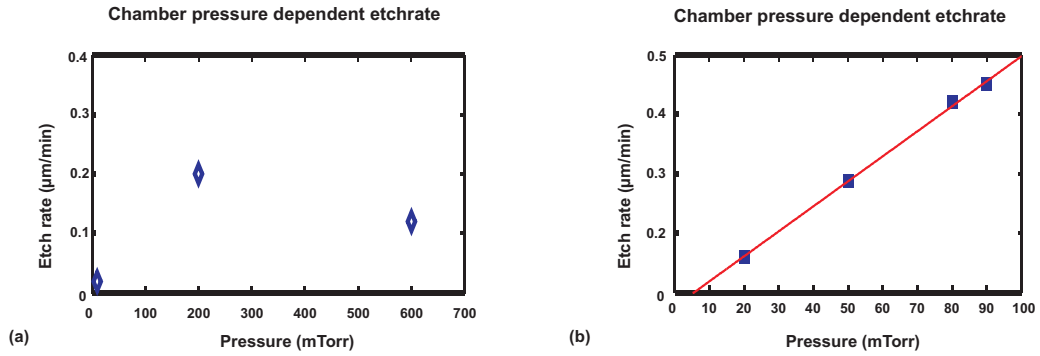


Figure 4.6: Etch rate of partially cured PI as a function of pressure in the chamber (a) The power applied is 20 W and the ratio of O_2/CF_4 is 85/15 in RIE (b) The power applied is 200 W, ratio of O_2/SF_6 is 80/20 and coil power is 2000 W in ICP

The third characterization step is to observe the change in the etch rate by changing the total gas flow (but keeping a constant ratio) in the chamber while other factors are kept constant. This has been done to characterize both systems i.e. RIE and ICP. In RIE the total gas flow (O_2+CF_4) was increased from 100 to 116 sccm and in ICP (O_2+SF_6) from 100 to 124 sccm. No significant change in the etch rate of PI was found in response to changes in total gas flow as shown in table 4.1.

Etching System	Platen Power (W)	Pressure (mTorr)	Total Gas flow (sccm)	Coil Power (W)	Etch Rate(μm/min)
ICP	200	80	124	2000	0.57
ICP	200	80	100	2000	0.52
Etching System	Platen Power (W)	Pressure (mTorr)	Total Gas flow (sccm)		Etch Rate(μm/min)
RIE	20	200	100		0.2
RIE	20	200	116		0.2

Table 4.1: The etch rate of PI in ICP and RIE with different gas flows

4.4 Best system for etching PI

The results of this step-wise optimization approach show that high power and high pressure can result in higher etch rates but at the same time it was observed that excessive heating of the quartz wafer occurs due to high ion bombardment on the surface of the substrate that causes the burnt residues in the bottom of the channel. To keep the heating of the substrate to a low level and still achieve a high etch rate the RIE system was preferred over the ICP system and was thereafter used as etching system for patterning microfluidic channels.

The best parameters chosen for etching partially cured PI were gas mixture of O_2 and CF_4 in a ratio 94:6, power of 100 W and pressure of 200 mTorr with achieved etch rate of 1.3 μm/min. These parameters were also tested on fully cured PI which was cured at 350℃ for 1 hr. It was found that the etch rate of fully cured PI is less than partially cured PI. Table 4.2 shows a summary of the optimized parameters for both fully and partially cured PI.

	Pressure	**Power**	**Gas Flow**		**Etch Rate**
	(mTorr)	(W)	(sccm)		(μm/min)
			O_2	CF_4	
Partially Cured PI	200	100	94	6	1.3
Fully Cured PI	200	100	94	6	0.55
Fully Cured PI	200	100	80	20	0.9

Table 4.2: Parameters used to etch partially cured PI and fully cured PI

4.5 Reproducibility of PI channel height

Three wafers were coated with 30μm thick PI by the multi-coating method and microfluidic channels were formed using the optimized etch recipe explained above. Five point profilometer measurements were done on these wafers to check the uniformity in the thickness and its reproducibility on all the wafers. The same microfluidic channels with 30μm height were also made in SU-8 and were compared with PI in terms of uniformity and reproducibility. Table 4.3 shows the data on mean thickness measurements of channel height with standard deviation for each wafer made in PI and SU8.

Wafer Number	SU8 mean thickness+standard deviation (μm)	PI mean thickness+standard deviation (μm)
W1	32.988+1.24	31.38+0.513
W2	34.35+1.285	31.29+0.352
W3	34.606+1.54	31.48+0.396

Table 4.3: Mean thickness measurements of channel's height along with standard deviation for each wafer made from SU8 and PI

From the data it is clear that PI has low deviation in the thickness of coating within a wafer compared to SU-8. Moreover, the reproducibility in the coating across 3 wafers is better in PI than SU-8. This experiment shows that PI is comparable to SU-8 in order to be used as an alternative material for microfluidics.

4.6 Closed channel microfluidics

Closed channel microfluidic systems were also made by bonding PI to PI and PI to glass. The microfluidic channels were made on the lower wafer in PI while the top wafer didn't have any pattern. Holes were milled in the quartz wafer for creating

an inlet and outlet for the fluid. The optimization of the parameters for bonding were also done by keeping the bonding temperature constant at 300℃ and adjusting the bonding time and force. The time was varied from 15 to 30 mins and the force was varied from 12 kN to 15 kN. Most of the bonding conditions resulted in the low yield of the bond as the air gap between two surfaces was quite visible due to poor bonding in many places on the bonded wafers and in some cases the channels were closed when the bonding time was increased. The optimal bonding conditions were found with 15 kN force, bonding time of 15 min for both PI-PI and PI-glass bonding. The SEM image of PI-bonded to glass is shown in figure 4.7.

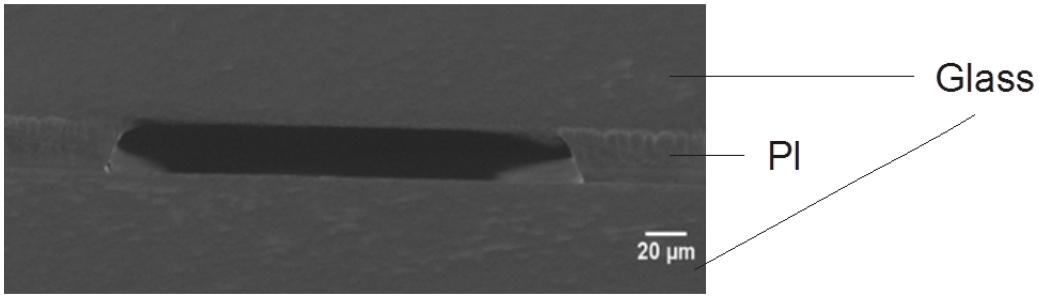


Figure 4.7: cross-sectional image of the closed-microfluidic channel formed by PI-glass bonding under scanning electron microscope

Two bond strength tests were performed to verify the durability of the channel. These tests are explained below:

4.6.1 Hydrodynamic focusing

Hydrodynamic focusing test was done as a first check for closed channel stability. As shown in figure 4.8 a blue colored fluid with a flow rate of 1μl/min from two sides joins a red colored fluid running with a flow rate of 2μl/min in the middle outlet of the channel and the resulting flow was observed under an inverted microscope.

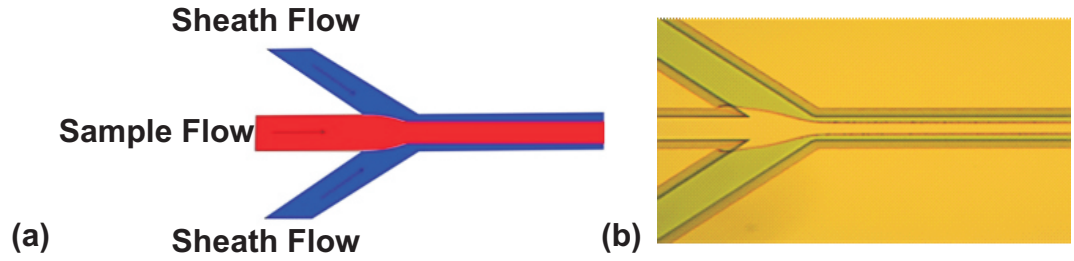


Figure 4.8: (a) Schematic diagram of hydrodynamic focusing of red colored fluid flowing at higher rate by using blue fluid flowing at lower rate (b) Image from inverted microscope of hydrodynamic focusing of red colored fluid flowing at 2μl/min with blue colored fluid flowing at 1μl/min

It was observed that both blue and red colored fluids followed the laminar flow even after mixing in the channel i.e. hydrodynamic focusing of red fluid was achieved and can be seen in the figure 4.8 b which indicates that a reliable bonding strength is maintained over the whole bonded interface. In figure 4.8 b the shadows appearing around the boundaries of the bonded channels are due to bending of the channel

during bonding that can also be seen in the SEM image in figure 4.7. However, this bending does not seem to be influencing the microfluidic system by the successful measurement made by hydrodynamic focusing.

4.6.2 Pressure drop test

As discussed in section 4.1, downscaling of microfluidics systems creates more fluidic pressure inside the channel and for a closed channel microfluidics system it is a major challenge to sustain such pressure levels. The closed channel microfluidics made by bonding PI-PI and PI-glass, were also tested for this aspect before implementing it on SiNW devices. For this reason, a pressure drop measurement setup was made as shown in figure 4.9.

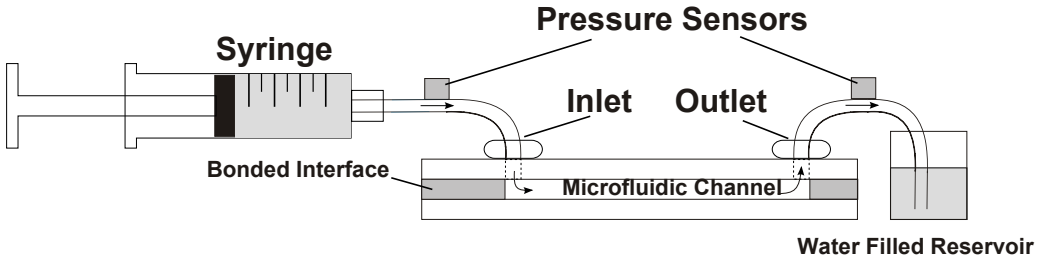


Figure 4.9: Schematic diagram of the setup used for pressure drop measurements

The setup consists of two gauge pressure sensors that are flush mounted at the inlet and outlet of the microfluidic channels. These pressure sensors are powered by a keithley sourcemeter and their output is connected to the PC via a DAQ card and interfaced with a Labview program. The measurement range of the pressure sensors is up to 250 psi/17.2 bars which is equivalent to the output voltage of around 140 mV. The calibration of these sensors is confirmed by using a compressed air source with an external gauge pressure sensor. In the LabVIEW program, the output of both the sensors is recorded simultaneously to observe the pressure drop across the microfluidic channel at different fluid flow rates due to possible deformation in the channel.

In pressure drop experiments, a linear behavior was observed within the test pressure range up to approximately 15 bars for both PI-PI and PI-glass bonded channels as shown in figure 4.10 with dimensions of $Length \times Width \times height = 3118 \times 77 \times 22.9$ μm and $length \times width \times height = 3118 \times 77 \times 11.6$ μm respectively. The flow rate was changed from 0.001 – 0.8 ml/min which is the range of flow rates most commonly used in microfluidic systems. These results are comparable to the findings by [93] where the fabrication process of forming closed microfluidic channel in flexible electronics is demonstrated. The hydraulic resistance of the channels was also extracted from these experiments and was compared with the theoretical values calculated by using Hagen-Poiseuille law for a rectangular channel with these dimensions. These values are depicted in the table 4.4

The experimental values match quite closely to the theoretical values which show that less deformation or delamination of bond occurs in this pressure range. Based on the bond strength test it was concluded that PI bonded channels are suitable for closed-channel microfluidics and can be implemented on SiNW based biosensors.

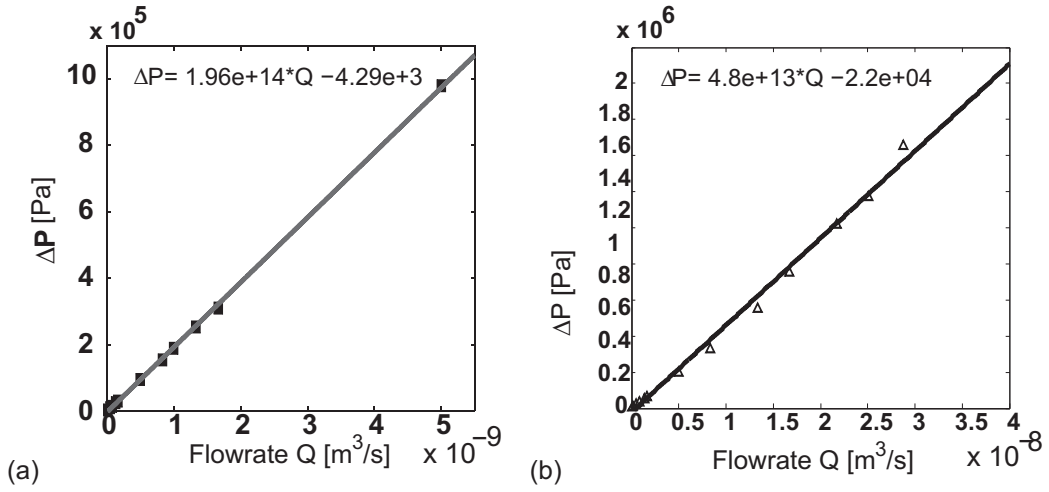


Figure 4.10: Pressure drop test after bonding (a) PI-PI bonded microfluidic channel with dimension $Length \times Width \times height = 3118 \times 77 \times 22.9$ μm (b) PI-glass bonded microfluidic channel with dimensions $length \times width \times height = 3118 \times 77 \times 11.6$ μm

Hydraulic resistance[Pa s/m^3]	PI-PI $3118 \times 77 \times 22.9$ (μm)	PI-Glass $3118 \times 77 \times 11.6$ (μm)
Theoretical value	4.98 $10^1$3	3.44 $10^1$3
Experimental value	4.82 $10^1$3	1.96 $10^1$4

Table 4.4: Comparison of hydraulic resistance values from experimental data with theoretical calculations

4.7 PI microfluidic integration with SiNW Bio-FET

After optimization of the fabrication process for forming microfluidic channels on quartz substrate, the next step is to integrate this process with the SiNW Bio-FET device fabrication process. There are two options to achieve this aim: one is to make the channels directly on top of SiNW and pattern them by dry etching and the other is to make the channels in quartz wafer and bond them to SiNW wafer to form closed channel. Since the functionalization protocol developed by the research group relies on open microfluidic channel, the first option was preferred, i.e. use PI as a passivation layer and microfluidic channel. For this reason the recipe developed by using both Si_3N_4 and Al mask with partially cured PI was used. The initial Bio-FET devices in PI were made by using Si_3N_4 as a mask. These devices demonstrated good results in the biosensing experiments as discussed in chapter 7 which provided the basis to make a shift from SU-8 to PI. However, the limitation for this process is that channel height of more than 10μm using this mask is not possible as fluorine based gases will etch away the mask. To overcome this limitation and to develop a standardize process for all channel heights; process by using Al mask was developed. During the testing of the devices two problems were observed after patterning the microfluidic channel on top of SiNW. The first problem was that during the etching of PI the surface roughness of PI was around 500 nm after etching 10μm of PI,

getting larger as the PI thickness increases. This results in non-uniform etching of PI and later some patches of PI are still left which can be seen on top of SiNW. The second problem was observed where the cross-linking of two SiNW was found by two probe measurements which is due to bad passivation properties of PI.

To overcome these problems, it was decided to fully cure the PI at 350℃ for 1 hr after spin coating which improves the passivation properties as advised by the supplier and then further optimize the recipe for etching PI to reduce the surface roughness during the etching process. Table 4.5 shows the optimized recipe that resulted in cleaner surface on top of SiNW

	Pressure	**Power**	**Gas Flow**			**Etch Rate**
	(mTorr)	(W)	(sccm)			(μm/min)
			O_2	CF_4	Ar	
Step 1	200	100	80	80	20	0.75
Step 2	Pump and purge					
Step 3	Pressure	Power	O_2	N_2	Ar	Etch rate
	200	100	80	20	20	0.5

Table 4.5: Recipe to etch fully cured PI with low surface roughness

The time for step 1 was adjusted based on the thickness of the PI and etch rate and the step 3 was set to remove last 1 µm of the PI without CF_4 because of its ability to etch the SiNW. This process recipe resulted in the absolutely clean surface on top of SiNW and also good passivation properties.

4.7.1 Closed Channel Microfluidic Channel on SiNW Bio-FET

The second option of forming closed channel microfluidics on top of SiNW was also studied. The fabrication steps are explained as follows:

- Microfluidic Channels are formed by etching partially cured PI with Al mask on a quartz wafer
- Before removing Al mask inlet, outlet and electrical contact openings were removed on the quartz wafer by laser micromachining.
- The Al mask was then removed from the quartz wafer followed by aligning to the SiNW Bio-FET wafer and bonding.

Figure 4.11 shows the optical image of SiNW Bio-FET after bonding and dicing

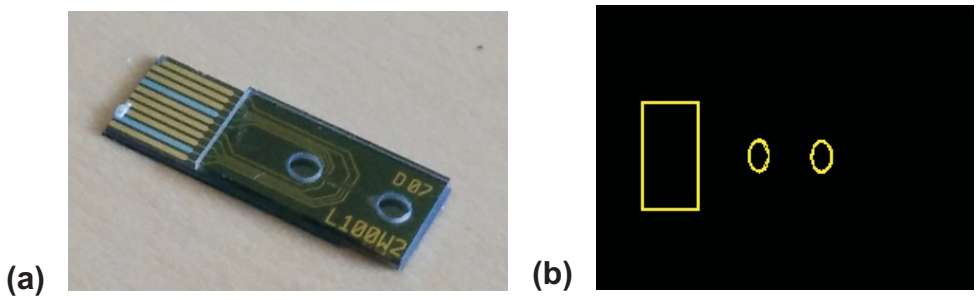


Figure 4.11: (a) SiNW Bio-FET sensor with closed microfluidic channel alongwith open inlet, outlet and electrical contacts (b) Auto cad image of inlet, outlet and contact openings used in laser micromachining

Chapter 5

Measurement Setups

In this chapter all the measurement setups are discussed that are used for characterization of SiNW Bio-FET and bio sensing experiments.

5.1 Setup for 1st Generation process

This measurement setup was developed by a former master student Micheal Jørgensen at NaBIS group. The setup consists of switching system in Faraday's cage, current pre-amplifier systems (Stanford research SR570), daq card (NI PCIe-6251) and PCI card for lab view (NI BNC-2111). These components work together in a way that the the daq card is connected to both the switching system (that switches source-drain from one SiNW to the other) and the current pre-amplifier. The outputs and inputs are controlled through lab view program via PCI card. The Faraday's cage contains switching system with the connections to the ZIF socket through data cable and as well as the microfluidics system on chip (with tubes for inlet and outlet of fluid on the SiNW) as shown in figure 5.1. In all the measurements made in this project the microfluidics within the switching system was not used. The top lid of the box was opened while making sensing experiments as the small amount of the liquids were pipetted directly on top of the SiNW chip. The rest of the connections

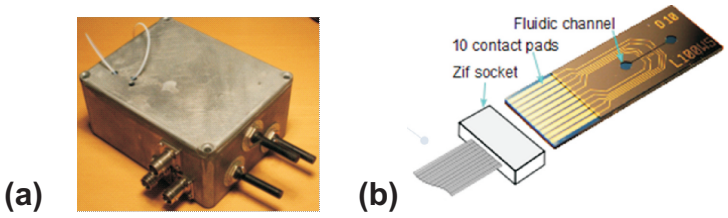


Figure 5.1: (a) Photo of switching system used to switch between four SiNW on one chip (b) Image of ZIF socket where the SiNW chips are inserted (taken from master's thesis).

in the measurement setup are shown in the figure 5.2. The impedance measurements on the SiNWs are made by applying voltage across SiNW through daq card port AO0 (the actual voltage is measured through AI0) and measuring the current from the SiNW using current pre-amplifier which converts it to the voltage and amplify the voltage to a level specified in the PC interface, this voltage is then communicated through the daq card port AI1and communicated to the lab view program.

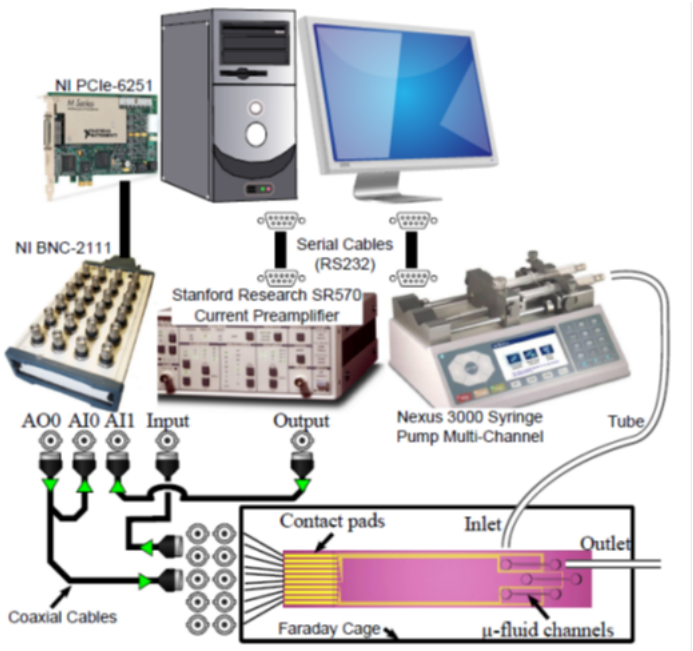


Figure 5.2: The measurement setup where the PC is connected to the current amplifier via PCI card and daq card. The co-axial cables from the amplifier are going to the switching box and to the daq card (master's thesis).

5.1.1 Impedance measurement of the SiNW

As a first step, the voltage and frequency to be applied across SiNW are specified in the LABVIEW user interface. In all the measurements, the voltage was set to 100 mV and frequency was set to 1 Hz which means measurements were made in DC volts. Figure 5.3 shows a screen shot of the LABVIEW interface. Then by

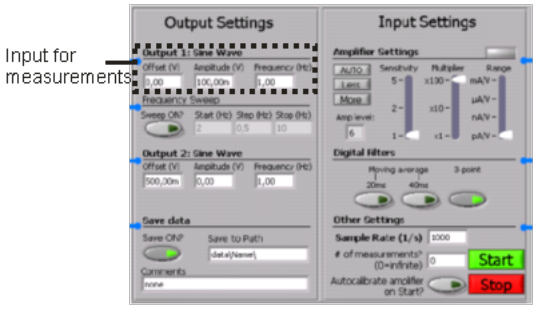


Figure 5.3: Screen shot of LABVIEW interface where the applied voltage and frequency and set on the labeled area (master's thesis)

pressing start button the program runs by acquiring the data from the connected pre-amplifier in which the signal has some noise as shown in step 1 in the figure 5.4. The digital filters shown in the figure 5.3 filters the noise from the signal which is shown in step 2 in figure 5.4. In step 3 the phase difference between voltage and current is determined. If there is no phase shift then the current and voltage signals are aligned in step 4. This aligned signal is then plotted as current vs voltage in step 5 with a linear fit. The reciprocal of the slop then gives us the modulus of the impedance. The LABVIEW program saves the impedance data as text file where each measurement is made after one second. The duration of measurements is set by

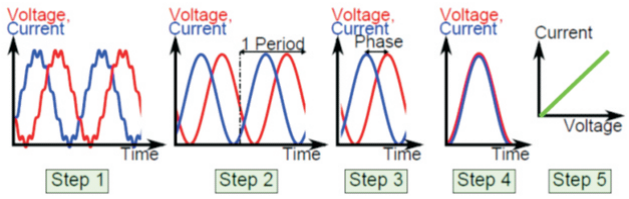


Figure 5.4: Different steps in the extraction of impedance from the raw signal implemented in LABVIEW

putting the time in seconds in the LABVIEW interface. The real time impedance value is shown on the interface as well. Figure 5.5 shows the screen shot of the measurements results.

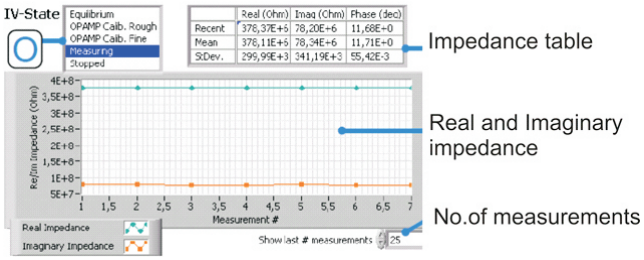


Figure 5.5: Screen shot of the LABVIEW interface with impedance display in table and as well as on the plot

5.2 CMOS Setup

The CMOS setup was provided by the EU Marie Curie project partner at ETHZ Basel. The purpose was to make a portable setup that can be transported to different partners where they can make detection at their laboratories. This CMOS setup is shown in the figure 5.6 The signal from the CMOS setup is communicated through

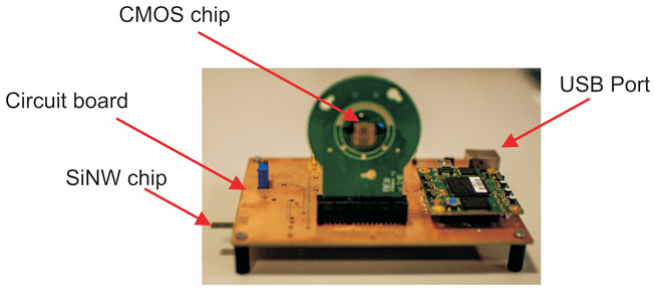


Figure 5.6: CMOS setup where the ZIF sockets are integrated with the circuit board connecting CMOS chip with SiNW

USB cable into the PC where the real time measurements are viewed and recorded at the interface made for running the setup.

The advantage of this setup compared to the 1st setup is that it is portable and it can record and display the data on all the four SiNWs at the same time.

5.3 Characterization Setup

The fabricated chips were characterized by inserting the chip in the ZIF socket soldered on the PCB board the cables for source and drain are also soldered on the PCB with different colors to differentiate between SiNWs connection. Figure 5.8 shows the image of the PCB board with SiNW chip inserted in the ZIF socket. The back gate is applied with the help of copper tape which sticks well on the back of the chip as shown in figure 5.7. The source-drain potential is applied by attaching

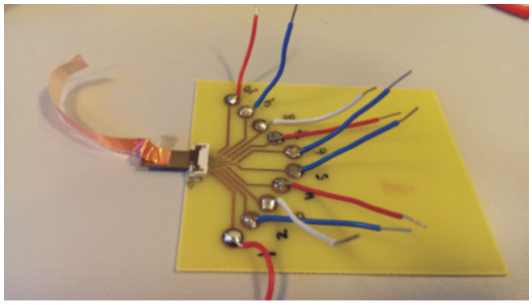


Figure 5.7: PCB board with ZIF socket and source-drain connections soldered on it. The SiNW chip has the copper tape stick to its back.

crocodile pins to the source and drain of each wire with specific color by using keithley source meter 2400. For back gate voltage the crocodile pin is attached to the copper wire and the voltage is applied with the help of another Keithley source meter 2400. The grounds of both the keithleys are connected together.

Both the keithleys are controlled through a LABVIEW program which applies and records the measurements of source-drain current and back gate leakage current at the same time and plots all the points in the real time as well.

Chapter 6

Electrical Characterization of Sensor

In this chapter, all the characterization techniques, used to ensure the reproducibility, high throughput and better functioning of SiNW-BioFET sensors, are discussed in detail. The first section explains the secondary ion mass spectroscopy technique that is used to count the number of dopants in the polysilicon after deposition. In the second section, the field effect characterization techniques for the SiNW Bio-FET device are explained. These give an idea of the sensor's response to the change in electrical field upon binding of the analytes onto the surface of functionalized SiNW. Thereafter, the electrical measurements done during different fabrication process steps are presented. These are used to trace any problems arising during the fabrication that can cause the malfunctioning of the device in the end. Lastly, the effect of annealing on the improvement of electrical behavior of the sensor is elucidated with the help of measurements.

6.1 Secondary Ion Mass Spectroscopy (SIMS)

The prime and most important factor for the correct function of the SiNW Bio-FET devices fabricated in this project is the in-situ doping of the polysilicon with the boron dopant concentration of around $3 - 5 \times 10^{18} atoms/cm^3$. This level of dopant concentration in polysilicon can potentially provide a better ohmic contact with metal as well as better sensitivity of SiNW for biosensing [79, 80]. While developing the recipe for in-situ doped polysilicon, the secondary ion mass spectroscopy (SIMS) technique was used to determine the concentration of boron atoms in the polysilicon thin film. Figure 6.1 shows the SIMS measurements on 50 nm thick in-situ doped polysilicon done immediately after deposition. The increase in the dopant concentration at the bottom of the polysilicon is due to the fact that according to the recipe use the furnace first releases diborane (B_2H_6) gas at a flow of 7 sccm for a few minutes and then releases the silane (SiH_4) gas. Several recipes were tried, where the B2H6 gas flow in the furnace was reduced from 7 sccm to 5 sccm and 3 sccm respectively, while keeping the SiH_4 gas flow constant. The SiNW Bio-FET devices were made by using polysilicon deposited by these recipes in the 1st generation process and tested in the measurement setup for 1st generation devices. A major capacitive behavior was seen in the impedance measurements, where a phase shift of more than 60° was measured. This was an indication of bad ohmic contact between metal and polysilicon due to low concentration of boron atoms. After this measurement SIMS measurements were not made on the polysilicon from these

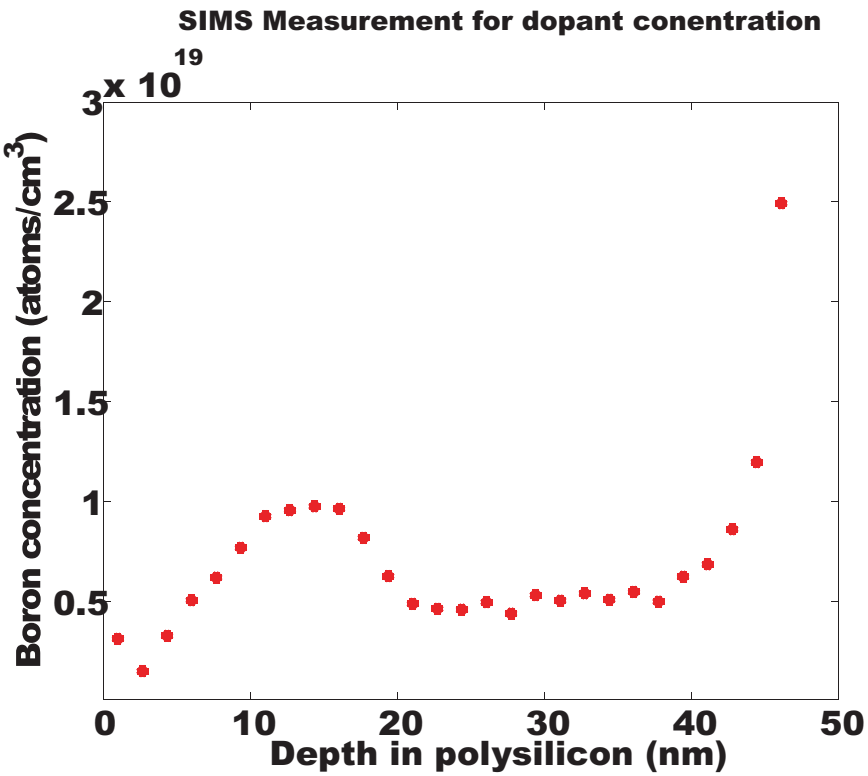


Figure 6.1: Dopants distribution within the in-situ doped polysilicon as measured by SIMS (where 0 is the top surface of the polysilicon and 50 is the bottom)

recipes.

Once an acceptable recipe was made and the Bio-FET devices were tested by the measurement setup, this recipe was used for the rest of the project. It was found later by using two probe electrical measurements (explained in section 3) that the dopants distribution was not the same all over the wafer. On the edges, the dopants concentration was higher compared to the center of the wafer, which could be due to the fact that while loading the wafer in the furnace, the boat is filled up with dummy wafers along with the test wafers in the rest of the slots due to which the center of the wafer is not exposed to the same amount of gas mixture as the edges are. This factor can be controlled by either leaving one slot empty between the two wafers in the boat or by giving a longer stabilization time for B_2H_6. But these changes were not tested during this project. The above measurement was done on the sample taken from the edge of the wafer.

6.2 Field Effect Characterization

After the fabrication of the SiNW device its electrical characterization is done, as a first step by keeping the source-drain voltage (V_{DS}) constant and sweeping the back-gate voltage (V_G) to monitor the change in source-drain current (I_{DS}) due to change in applied electrical field and as a second step by keeping the V_G to different constant potentials and sweeping the V_{DS} to observe the change in I_{DS} at each back gate potential. Through these electrical characterization techniques we can extract the main characteristics of the SiNW such as mobility of carriers, threshold voltage,

accumulation mode, depletion mode and trans-conductance.

In this section, the electrical characterization data of all generation processes are explained in detail by extracting the main characteristics of the SiNW.

6.2.1 Removal of side gate

The earlier devices, made by the 1st generation process, experienced the problem of source-drain connection loss during functionalization. Further investigations revealed that galvanic corrosion occurs at the very first step of functionalization by hydrosilylation method (explained in chapter 7), where the native silicon oxide is removed from the surface of the SiNW with hydrofluoric acid (HF). The side gate, which is made of Au and is designed to be right next to the SiNW in the microfluidic channel (about 2μm away from the wire), acts as cathode and the p-type SiNW acts as an anode due to their different rest potentials. In the presence of fluorine ions, polysilicon is removed in an oxidation reaction. The reaction is boosted by the presence of excess holes in p-type silicon as well as by light induced creation of electron-hole pairs, increasing the etch rate further. This phenomenon was verified through literature [103, 104]which led to the removal of the side gate electrode in Au from the sensor design. Figure 6.2 shows the real time measurements made on SiNW.

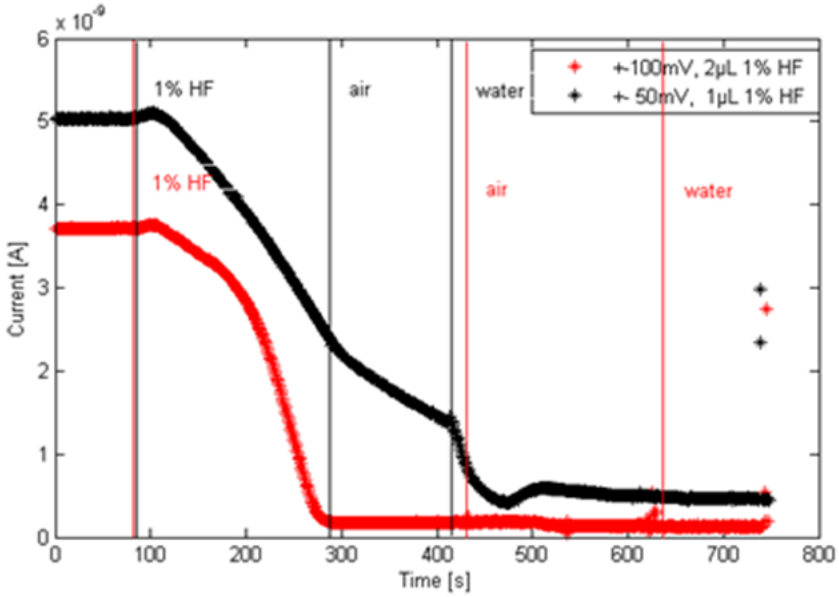


Figure 6.2: Real time measurement of oxide removal and corrosion of polysilicon in 1% HF solution in a flow cell at a flowrate of 0.5μL/min. The graph shows the peak current recorded at a slow alternating voltage (1Hz) at the amplitude indicated (50 mV and 100 mV). The decrease in current over time indicates the successive removal of polysilicon from the nanowire and eventually leads to breakdown of connectivity (courtesy of Andrea Pfreundt)

6.2.2 Electrical characterization of first generation process

The electrical characterization is done by using the setup explained in chapter 5. The devices fabricated by the 1st generation process with the following specifications

were characterized first. Table 6.1 shows the device specifications by first generation process

SiNW thickness	54 nm
Buried Oxide thickness	170 nm
Metal electrodes (Cr/Au)	20 /100 nm
PI microfluidic channel	10μm

Table 6.1: Specifications of SiNW Bio-FET made by 1st generation process

Figure 6.3 shows the field effect behavior of all the SiNWs in one chip when the back gate was swept from -40V to +40V while keeping the source-drain potential (V_{DS}) constant at 1 V and 0.3 V. The reason to choose 1V as V_{DS} was to observe a high change in source-drain current (I_{DS}) at each incremental step in back gate voltage (V_G) while 0.3 V V_{DS} is used to extract the mobility constant and doping concentration in the SiNW and also to provide a better estimation of the SiNW behavior at low potentials since the sensing experiments are made at low potentials. From figure 6.3 it is clear that all the SiNW on the same chip behave similarly and

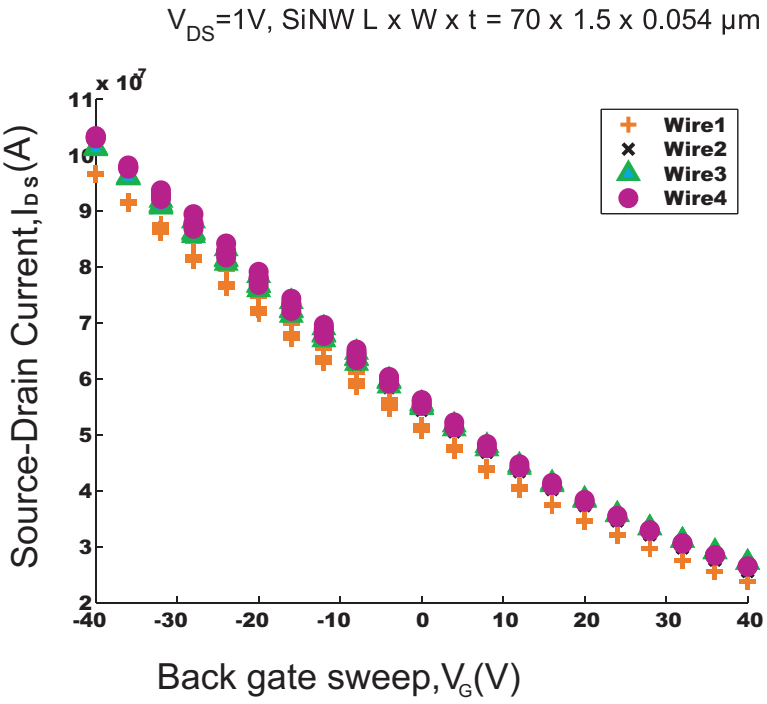


Figure 6.3: The change in source-drain current (I_{DS}) of all the four SiNWs with dimensions $L \times W \times t = 70 \times 1.5 \times 0.054\mu$m while sweeping the back-gate potential from -40 – +40 V when V_{DS} is set to 1V on one chip

they can be gated by the back gate, however, the effect is not large and full depletion cannot be achieved. In this plots, each point is a mean value of around 15 recorded points that are made during 2 seconds of measurements at each step.

After the fabrication of the wafers by all generation processes, the first test to see the significant effect of the back gate potential in the SiNW current, the source drain potential V_{DS} was set at at 1 V. Once the field effect behavior was confirmed

then the measurements were made at 0.3 V to extract the transfer characteristics of the SiNW as 1V is too high for such a small SiNW.

Since the SiNW Bio-FET acts like a resistor, its ohmic behavior was also tested by measuring the current (I_{DS}) vs voltage (V_{DS}) characteristics of the SiNW at different back gate voltages. Figure 6.4 shows the I_{DS} vs V_{DS} plot of the SiNWs fabricated by 1st generation process.

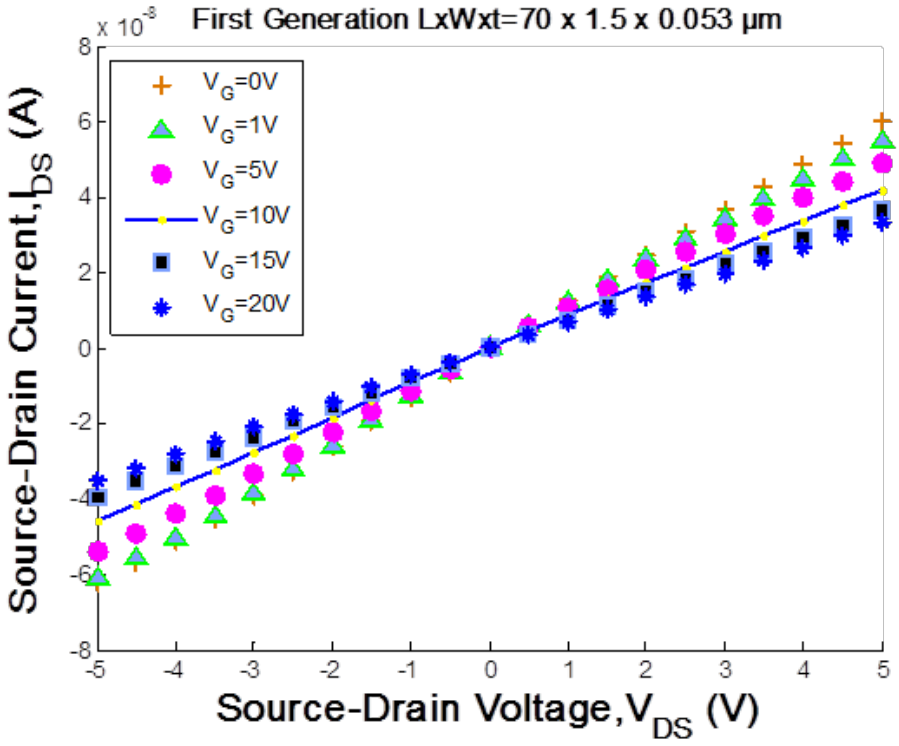


Figure 6.4: The source-drain current (I_{DS}) as function of source-drain potential (V_{DS}) at different back gate potential (V_G)

It can be seen that the effect of the back gate is minimal and that the nanowire behaves very linearly even at high source-drain voltages, indicating a largely ohmic behavior.

The main characteristics of the SiNW Bio-FET device can be extracted using these I-V curves.

6.2.2.1 Mobility constant extraction

The slope of the curve from I_{DS} vs V_G in accumulation mode was used to extract the mobility of the charge carriers by putting its value in equation 2.37 derived in chapter 2, i.e.

$$\mu_p = \frac{Lt_{ox}}{W\epsilon_{ox}V_{DS}}\alpha \tag{6.1}$$

Where μ_p is the mobility constant, L is the length of the SiNW, t_ox is the thickness of the buried oxide, W is the width of the SiNW, ϵ_{ox} is the dielectric constant of oxide, V_{DS} is the source-drain potential and α is the slope of the I-V curve.

The mobility of the charge carriers was calculated for all the wires and was found to be around $1.0328 cm^2/Vs$ which is in close agreement with literature [105,

106]. The mobility of the polycrystalline is dependent on the grain size and dopant concentration [105, 106]. This low mobility is due to small grain size as observed during the fabrication process shown in figure 3.10 and high dopant concentration. This also explains the ohmic behavior of figure 6.4.

6.2.2.2 Doping concentration extraction

As mentioned earlier, the dopants distribution was not the same all over the wafer. The I-V curves produced above were plotted from the data acquired from the device taken from the center of the wafer. By using the I-V curve again we can use equation 2.38, explained in chapter 2, to calculate the dopant concentration.

$$p_0 = \frac{KL}{W\mu_p qtV_{DS}}\alpha \tag{6.2}$$

Where p_0 is the dopant concentration, K is the source drain current at 0 back gate voltage V_{DS} is the source drain voltage, t is the thickness, L is the length and W is the width of the SiNW. The dopant concentration after putting all the values was calculated to be $8.762 \times 10^17 atoms/cm^3$. This dopant concentration shows that the effective number of dopants involved in the conduction process is lower than the number of dopants measured through SIMS. It means that not all the dopants were activated and this led to the inclusion of annealing step in 2nd and 3rd generation.

6.2.2.3 Conclusion

It can be seen from the measurement results that the complete depletion of the wires was not achieved even by going high up to +40V in back gate potential. Similarly, the change in I_{DS} as a function of V_{DS} by changing the back gate is found to be very low. After the electrical characterization of these devices, they were also tested for bio sensing which is discussed in chapter 7 in detail.

Based on the findings from 1st generation process electrical characterization and bio sensing experiments the list of improvements were made in fabrication process as explained in chapter 3 for 2nd generation process.

6.2.3 Electrical characterization of 2nd generation process

The electrical characterization of the 2nd generation process was also done by using the same setup as that of 1st generation process. Table 6.2 shows the basic specifications of the devices made by the 2nd generation process.

SiNW thickness	35 nm
Buried Nitride	thickness 54 nm
Metal electrodes (Cr/Au)	20 /100 nm
PI microfluidic channel	10μm

Table 6.2: Specifications of SiNW Bio-FET made by the 2nd generation process

Figure 6.5 shows the I-V curves obtained by sweeping the back gate potential from -15 V - +15 V for a 35 nm thick SiNW.

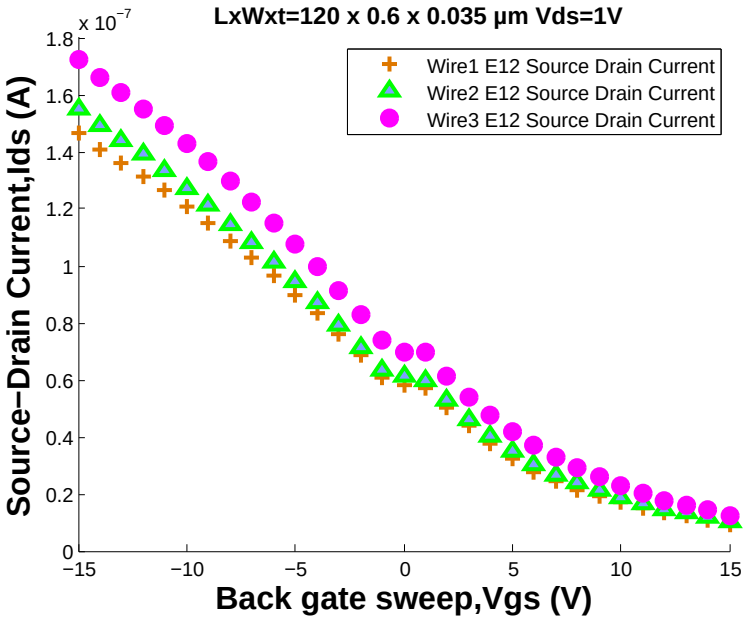


Figure 6.5: The change in source-drain current (I_{DS})all the four SiNWs with dimensions $L \times W \times t = 120 \times 0.6 \times 0.035\mu$m while sweeping the back-gate potential V_G from -15 – +15 V when V_{DS} is set to 1V after fabrication by 2nd generation process

It was not possible to apply more than +15 V to the back gate as the leakage current through the buried nitride increases dramatically beyond this limit and affects the I_{DS}. The leakage current as a function of back gate potential is shown in figure 6.6. Theoretically the 54 nm thick nitride layer should be able to withstand at least 54 V (based on the dielectric strength measurements) but this is not practically the case. One of the factors influencing this low insulation strength was found to be the dislocations in Si_3N_4 at the Si/Si_3N_4 interface [87]at high temperatures due to difference in thermal co-efficient of both the materials. It should be noted that the leakage current measured at 20 V back gate is still one order of magnitude smaller than the I_{DS} current, so that only 10% of the current goes through the isolation layer. However, we stopped the measurements at 15 V.

From this point onwards, the leakage from back gate was added as a standardize test along with the I_{DS} vs V_G at V_{DS} of 1V after the fabrication of the Bio-FET devices.

6.2.3.1 Mobility constant and dopant concentration

By using the slope of the IDS-VG curve and putting it in first equation, the mobility was calculated as $0.408cm^2/Vs$. Applying this value of mobility in equation 2.38 the dopant concentration was calculated as $3.465 \times 10^19 atoms/cm^3$. The reduction of the mobility was not in accordance to the hypothesis we made before fabrication of the devices by 2nd generation. But after going through the whole process and calculation results following factors were found to be involved in this result.

- The first factor was that the concentration of dopants got higher when the thickness was reduced from 54 nm to 35 nm. It was due to the fact discussed earlier in SIMS measurements that in the furnace process B_2H_6 is released first for some time before releasing SiH_4 and from SIMS measurements it was

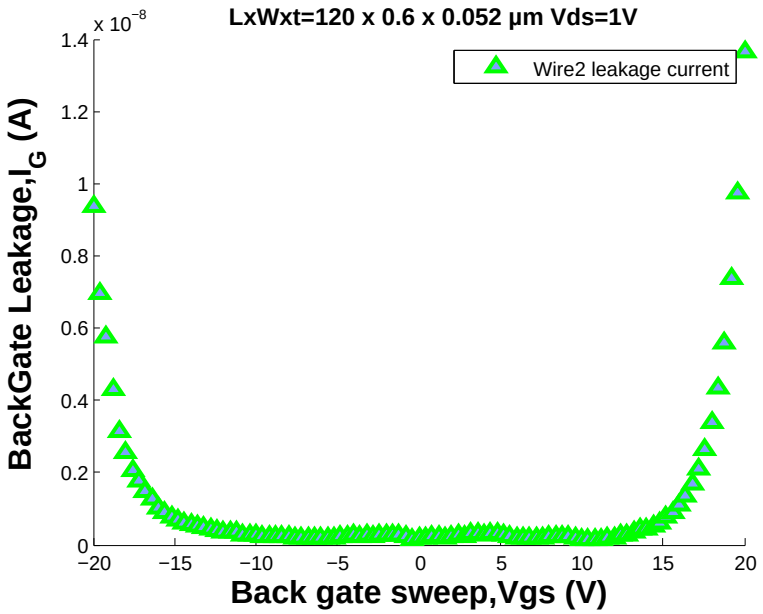


Figure 6.6: Back gate leakage current I_G as a function of V_G after 2nd generation process

also clear. In this case, the thickness was grown to only 35 nm which resulted in high dopant concentration and the annealing step at 900℃ for 30 mins activated most of the dopants that are involved in the conduction process.

- The other factor was the failure in changing the grain size of the polysilicon. Following the SEM picture made in figure 3.10 the grain size was unchanged by treating at 900℃ for 30 mins.

6.2.3.2 Conclusion

The slope of the I_{DS} vs V_G was improved in 2nd generation process which was seen by the increased effect of back gate potential in figure 6.5 mainly due to the reduction of the thickness from 54 nm to 35 nm but still the complete depletion of SiNW was not achieved. The mobility on the other hand decreased due to small grain size and increase in the dopant concentration. These Bio-FET devices were also used for bio sensing experiment of NKG2D cancer biomarker detection as discussed in chapter 7.

The improvement of the mobility by increasing the grain size and reducing the dopant concentration was considered along with the reduction of the thickness of the SiNW in the process that led to the formation of the 3rd generation process with improved electrical performance. The significant changes made in the fabrication process are discussed in chapter 3.

6.2.4 Electrical characterization of 3rd generation process

The devices made by 3rd generation process were also characterized electrically. Figure 6.7 shows the I_{DS} vs V_G curve obtained by the measurement setup.

From the figure it is clear that the complete depletion in SiNW was achieved at around 5 V in Figure 6.7. Since the dopant concentration is not the same all over

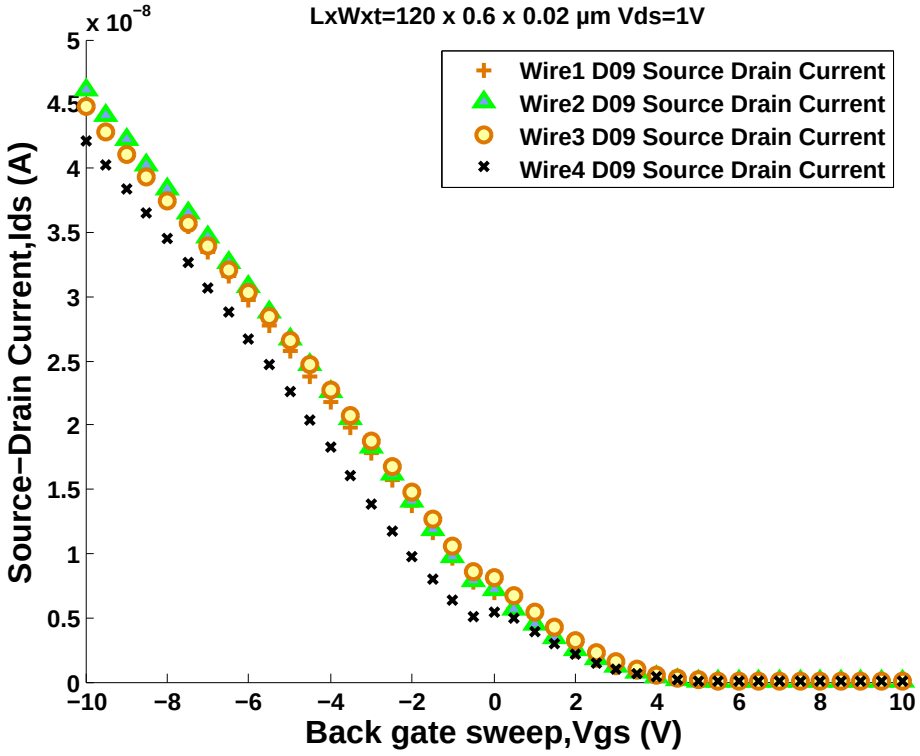


Figure 6.7: The change in source-drain current (I_{DS})for all the four SiNWs with dimensions $L \times W \times t = 120 \times 0.6 \times 0.02\mu$m while sweeping the back-gate potential from -10 – +10 V when V_{DS} is set to 1V after fabrication by 3rd generation process

the wafer, the voltage needed to completely deplete the SiNW varies between 5-10 V. In the above mentioned case the devcie was taken from the center of the wafer which has less dopant concentration.

The back gate leakage characterization as shown in figure 6.8 also showed the improvement in the insulation property of the buried insulator due to the fact that 30 nm dry oxide was added between Si/Si_3N_4 interface.

This insulation property could be improved further by increasing the thickness of oxide but then a higher back gate potential will be required to deplete the SiNW. Since we have to make sensing at sub-threshold regime and to use the device in the Point-Of-Care (POC) setup low back gate voltages are preferred.

6.2.4.1 Mobility and dopant concentration

Since the buried nitride has been replaced by the stack of SiO_2 and Si_3N_4 layer the capacitance per area was recalculated where the two layers are connected in series. According to equation 2.36 from chapter 2

$$\alpha = \frac{W\mu_p C^*_{ox}}{L} V_{DS} \tag{6.3}$$

From this equation μ_p can be written as

$$\mu_p = \frac{L\alpha}{WC^*_{ox}V_{DS}} \tag{6.4}$$

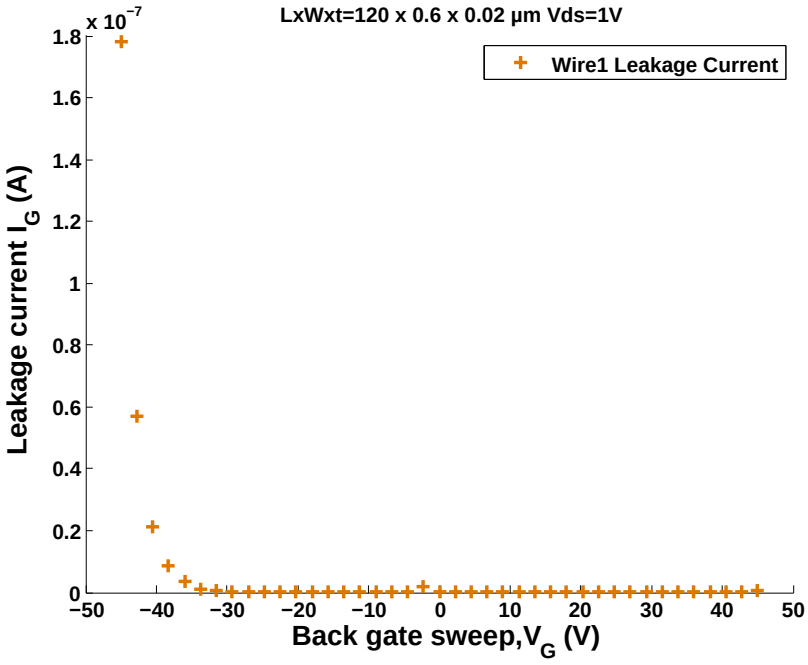


Figure 6.8: Leakage current I_G as a function of back gate V_G swept from -45 V - +45 V on the SiNW after 3rd generation process

where $C^*_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ But for a buried insulator having SiO_2 and Si_3N_4, C^*_{ox} will have to be modified as

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{nit}}\frac{1}{C} = \frac{t_{ox}}{\epsilon_{ox}\epsilon_0 A} + \frac{1}{\epsilon_{nit}\epsilon_0 A} \tag{6.5}$$

deriving the above equation to get $C/A = C'$ gives $C' = 6.09 \times 10^{-4} F/m^2$

Now using these values in equation 2.37 the mobility was found to be $3.594 cm^2/Vs$ and dopant concentration was obtained to be $7.55 \times 10^17 atoms/cm^3$. The increase in the mobility is due to the fact that grain size has been increased (grain size was not possible to measure in SEM anymore due to a lot of discharging) and can be inferred from the SEM image in figure 3.12b and at the same time reduction in the dopant concentration. This process change has proved the hypothesis which results in the better sensitivity of SiNW.

The voltage controlled resistance characterization of these SiNW was also done. Figure 6.9 depicts the change in I_{DS} at different back gate voltages when the V_{DS} is varied.

From the figure 6.9 it was observed that the gating effect has a bigger influence on the resistance of the SiNW, but at the same time on the –ve V_{DS} the saturation was not achieved as compared to the characterization results achieved by Lieber's group [63]. The trouble shooting was done on the measurement setup and it was observed that the source to gate potential was not referenced to the same ground and there is some kind of loop that exists between the two grounds (highlighted in red in figure 6.10 when the polarity of the source is changed. Figure 6.10 shows the schematic of the connections in the measurement setup.

To confirm the problem in the measurement setup one of the chip was characterized in the semiconductor analyzer equipment by Agilant.Figure 6.11 shows the I_{DS} vs V_{DS} curve for 3rd generation device measured by Agilant.

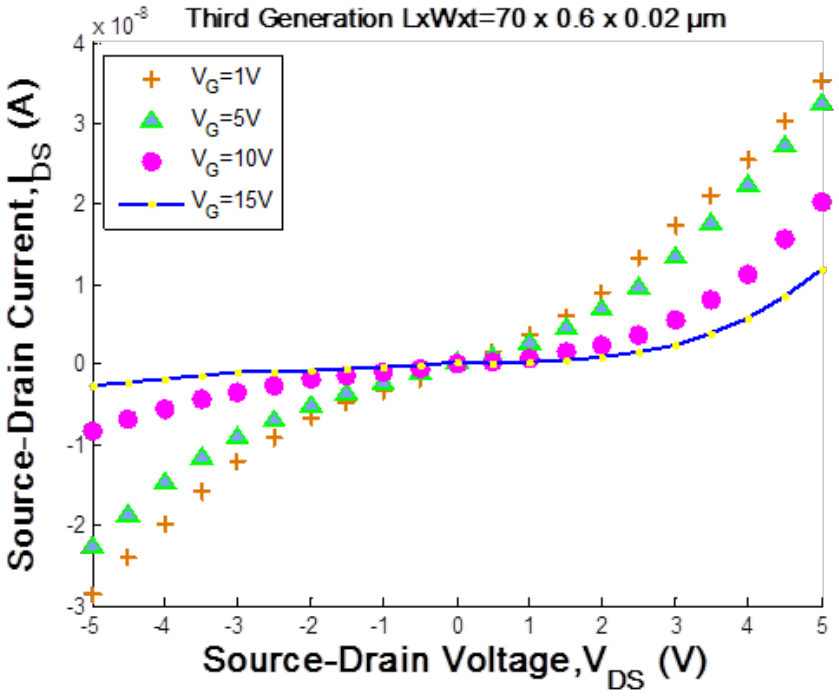


Figure 6.9: The source-drain current (I_{DS}) as function of source-drain potential (V_{DS}) at different back gate potential (V_G)

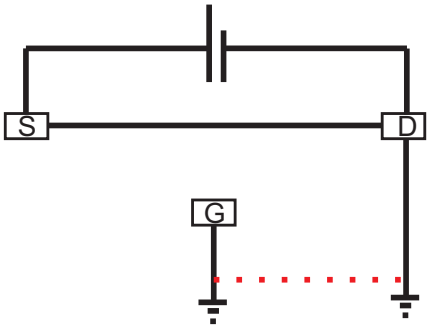


Figure 6.10: Schematic diagram of the connections in the setup. The possible leakage is coming from the loop between two grounds highlighted in red.

6.2.4.2 Conclusion

From the electrical characterization results of 3rd generation, we can claim that a better sensitive SiNW has been fabricated by using novel in-situ doped polysilicon which has the same characteristics as that of the devices made by Lieber's group [63]. Further, bio sensing on this generation devices are under progress

6.3 Two probe electrical measurements

As during the fabrication of the 1st and 2nd generation devices there were a lot of nanowires with no source-drain contact for reasons that we could not understood, we decided to troubleshoot the process by performing electrical measurements to verify the contact after each relevant process step. The results were used in order

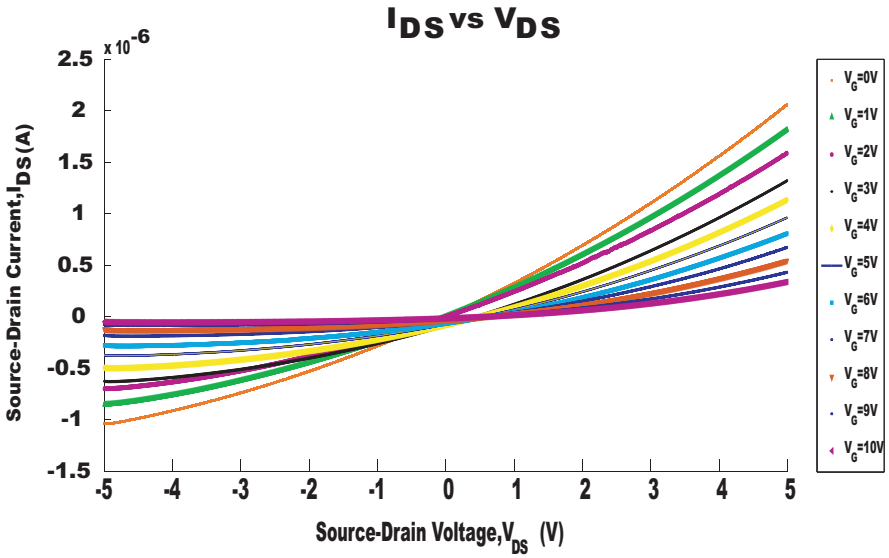


Figure 6.11: The source-drain current (I_{DS}) as function of source-drain potential (V_{DS}) at different back gate potential (V_G)

to improve the process (e.g. replace the PI passivation layer with sputtered nitride) and improve the contacts.

In the following sections the observations made at each step during fabrication of 3rd generation devices are presented.

6.3.1 After polysilicon deposition

Two probe measurements were done at 5 points on the 4 inch wafer after the in-situ doped polysilicon deposition, where the distance between the probes was kept to 550μm. Table 6.3 shows the measurements made at different places on the wafer.

Location on the wafer	Resistance Measurement (Ω)
Top	143 K
Center	470 K
Bottom	108 K
Right	119 K
Left	72 K

Table 6.3: Two probes measurement at five locations on the wafer after 28 nm thick deposition of polysilicon

From the measurements, it is clear that the dopants are not uniformly distributed across the wafer. The center of the wafer has a lower dopant concentration than the edges.

6.3.2 After oxidation and annealing

Similarly, the measurements were made after dry oxidation of 1 min and 20 mins annealing at 1100℃, while keeping the distance between the probes to 550μm. Table 6.4 shows the measurements made at different places on the wafer.

Location on the wafer	Resistance Measurement (Ω)
Top	200 K
Center	300 K
Bottom	68 K
Right	109 K
Left	78 K

Table 6.4: Two probes measurement at five locations on the wafer after oxidation and annealing on 20 nm thick polysilicon

The measurements show that some re-distribution of dopants occurs after this process but not a significant difference is observed across the wafer. However, it confirms that the high temperature oxidation is not at this point responsible for loss of contact.

6.3.3 After Electrode deposition

The next measurement was made after metal deposition of TiW and Au to check the resistance across source-drain contacts. Table 6.5 shows the resistance measured on four SiNWs on the same chip. From the measurements it is observed that in some

Chip Name ($L \times W = 70 \times 0.6\mu$m)	Resistance Wire1(MΩ)	Resistance Wire2(MΩ)	Resistance Wire3(MΩ)	Resistance Wire4(MΩ)
B01	100	90	X	160
B05	155	160	X	153
B09	156	159	84	X
C04	X	185	177	168
C08	180	184	183	174
C12	162	152	160	132
D03	X	X	194	190
D07	X	X	180	192
D11	88	89	159	160
E02	X	X	X	X
E06	175	171	191	166
E10	158	173	127	139

Table 6.5: Two probes measurement on four SiNWs of three chips on each column of the wafer

of the wires there were no connections (as indicated by X). At the same time the wires with the connections had a lot of drift in the resistance values and there was a big difference in the resistance values on each of the four wires on the same chip

6.3.4 After Contact annealing

To improve the contact and stability in the resistance values the annealing step was made at 350℃ for 1 hour. The two probes measurements on the same chips were made after annealing. Table 6.6 shows the resistance measurements after contact annealing.

Chip Name ($L \times W = 70 \times 0.6\mu$m)	Resistance Wire1(MΩ)	Resistance Wire2(MΩ)	Resistance Wire3(MΩ)	Resistance Wire4(MΩ)
B01	48.4	47.25	52.8	61.2
B05	44.42	45.9	X	49
B09	39.6	38.4	38.2	63
C04	108.2	100.6	102.4	90.06
C08	72.65	77.5	87.8	87.6
C12	48	41.6	40.02	41.04
D03	94.5	93.1	96.5	102.2
D07	101.1	82.1	83.6	107.3
D11	46.1	45.8	57.3	64.18
E02	177	143	127.5	X
E06	63.5	51.2	68.2	62.3
E10	51.7	54.5	50.6	50.2

Table 6.6: Two probes measurement on four SiNW of three chips on each column of the wafer after contact annealing

The above measurements showed that the contact between metal and polysilicon was improved significantly and more stable resistance values were recorded. Moreover, the difference in the resistance value between the four wires on each chip was also reduced. Some SiNW that were not giving connection in the earlier step also got the connection. After this step the yield of the fabrication process increased significantly.

Figure 6.12 shows the distribution of resistances before and after contact annealing based on the measurements on all the SiNWs on one wafer during fabrication process. The figure clearly shows the trend of improvement in the contact resistance

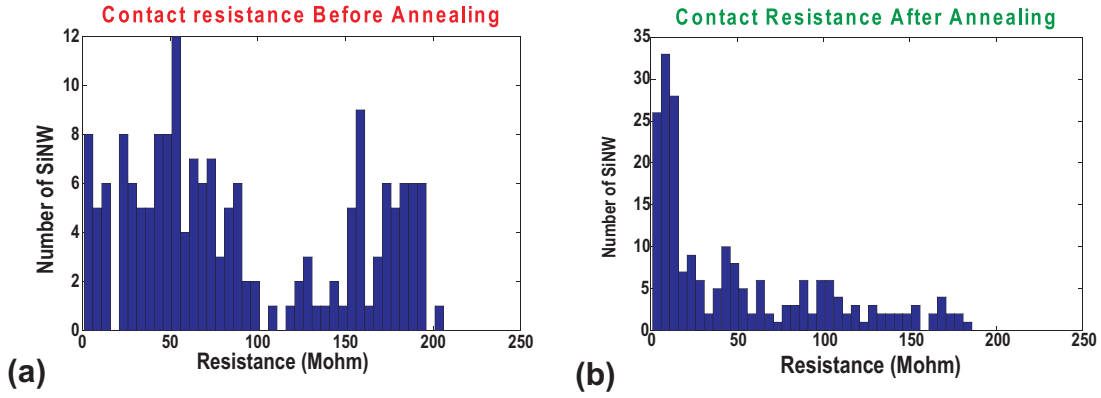


Figure 6.12: The trend of contact resistance between SiNW and Au before and after annealing

between Si and metal.

6.3.5 Passivation by sputtered Si_3N_4

The recipe for the sputtered Si_3N_4 was also optimized. A Si target was used and by changing the ratio of Ar to N_2 in the plasma, the dielectric strength was improved.

Table 6.7 shows the parameters used for deposition. The dielectric strength tests were made after the deposition of nitride layer by each recipe.

Gas ratio	Power (W)	RF Power (W)	Dielectric strength (V/nm)
Ar 10% of N_2	90	10	0.25
Ar 25% of N_2	90	10	0.65

Table 6.7: Dielectric strength of sputtered Si_3N_4 at different Ar:N_2 ratio

The resistance measurements were made on the SiNW after sputtering as well but no significant change was observed.

6.4 Conclusion

Based on all the electrical characterization measurements made on the devices fabricated by all three generation processes, it is concluded that the SiNW Bio-FET devices made by the 3rd generation process have the best sensitivity to external applied field, which means that their response to the field effect produced by the biomolecules will be higher compared to the devices made by other generation processes. These structures were the only ones that could be fully depleted at relatively low gate voltages (maximum 4 V), which is also desirable since the device is to be used in a Point-of-Care setting, where low power consumption is necessary.

The magnetron sputtered TiW doesn't have good adhesion to the SiNW contact pads and requires RF cleaning step but it acts as a good diffusion barrier layer for Au. The contact annealing greatly improved the metal to silicon contact. The dielectric strength of sputtered nitride is good enough to provide passivation of gold electrodes. Use of sputtered nitride instead of PI, which was also serving the purpose of functioning as a microfluidic channel, means that a separate microfluidic channel needs to be fabricated e.g. in PDMS and aligned to the chip outside the cleanroom. Such structures were fabricated by PhD student Andrea Pfreundt (also part of EngCaBra) and were shown to function very well.

Chapter 7

Biosensing

In this chapter all the experiments done on SiNW Bio-FET devices for biomolecules sensing are explained and discussed in detail. The first section briefly describes the functionalization procedures that were used to modify the surface of the SiNW to enable binding of the biomolecules on the surface. In the later sections, the sensing experiments carried out by using 1st and 2nd generation devices are described. Lastly, the pH sensing experiment using 3rd generation process is elucidated.

7.1 Functionalization of SiNW

The surface functionalization of the SiNW is carried out by surface chemistry techniques that use either the native oxide on SiNW surface (process known as silanization) or the bare Si surface by removing the native oxide (process termed as hydrosilylation). By using these methods, an affinity layer is formed on top of SiNW that interacts with the analyte of interest. The functionalization protocols used in this project are developed by PhD student Andrea Pfreundt from the NaBIS group and a Post Doc Lars Andresen from the University of Copenhagen.

7.1.1 Silanization Method

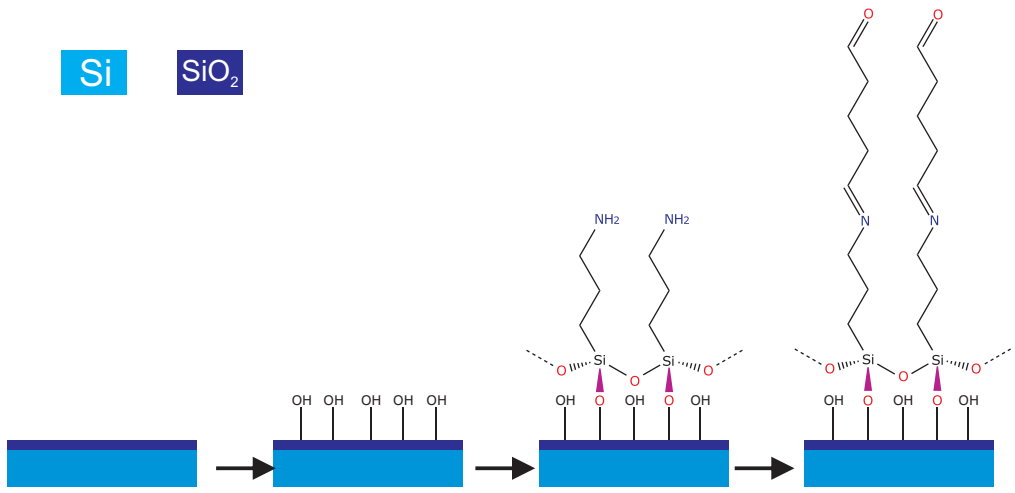


Figure 7.1: Schematic diagram of functionalization steps with APTES (the cross-linker in this case is Glutaraldehyde)

In this method, firstly the oxide surface of SiNW is changed to –OH terminated surface by cleaning the device in pure ethanol followed by exposure to oxygen plasma (the detailed recipe can be found in the appendix). Thereafter, the organosilane 3-Aminopropyl-triethoxysilaneis (APTES) is covalently bonded to the SiNW, which forms a monolayer and turns the surface of SiNW to a $-NH_2$ terminated surface. This surface has now affinity to bind with biomolecules like proteins, antibodies etc. To ensure the stability in the binding of biomolecule to the APTES, a cross-linker is also added to the APTES which can have $-NH_2$ or –COOH terminator depending on the configuration of the target biomolecule. Figure 7.1 shows the schematic of the functionalization steps.

7.1.2 Hydrosilylation Method

By this method an –H terminated surface on Si is produced by etching away the native oxide. The surface is then turned to an –alkyne terminated surface by incubating it in alkyne solution in the presence of UV light and absence of oxygen and moisture for longer time. The monolayer formed in this way is quite stable and does not need the cross-linker. The binding event of protein, e.g. antibody, takes place when the protein is first conjugated with an azide and then chemically reacted with the alkyne layer in the presence of Copper ions Cu (I) that catalyze the process. This coupling process of antibody to alkyne terminated surface is also called click-chemistry. Figure 7.2 shows the schematic diagram of functionalization steps by Hydrosilylation method.

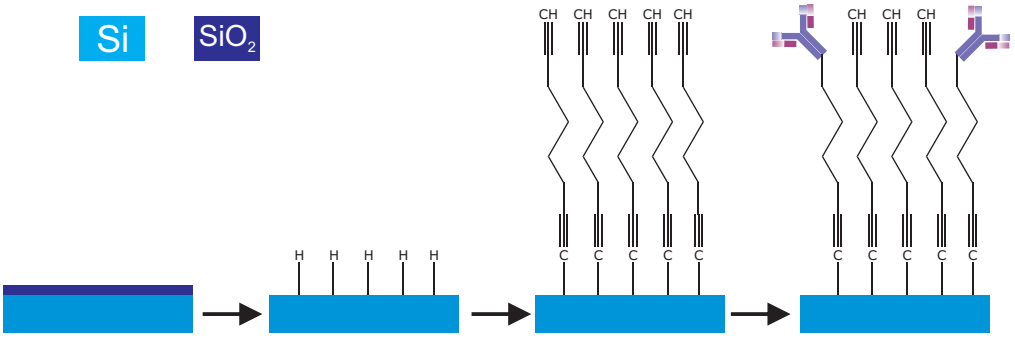


Figure 7.2: Schematic diagram of functionalization steps by Hydrosilylation method where alkyne terminated surface (in this case 1,7 Octadiyne) is formed on SiNW followed by antibody attachment by click chemistry

7.2 Bio-sensing with 1st generation process devices

After the fabrication of devices by 1st generation process, the bio-sensing experiments were done using both the silanization and the hydrosilylation method for functionalizing the SiNW. Two biological assays were performed using these devices, namely antibody-antigen detection and DNA hybridization. The DNA hybridization detection was done by using silanization while the antibody-antigen binding system was tested using hydrosilylation method. These sensing experiments are explained below in chronological order.

7.2.1 Primary-Secondary antibody binding detection

Binding of primary to secondary antibody concept is used for various in vitro immunological assays. This binding system was used to test the very first working prototype of Bio-FET devices produced by 1st generation process.

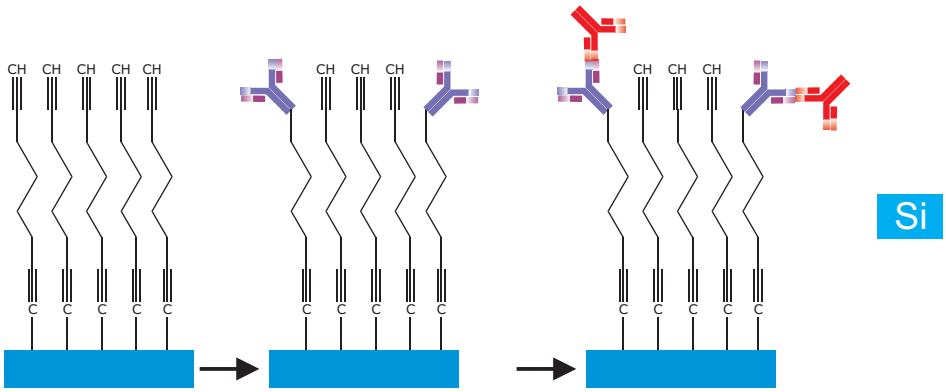


Figure 7.3: Schematic diagram of the steps used to detect secondary antibody by utilizing hydrosilylation method to functionalize the surface of SiNW with primary antibody.

In this sensing experiment, the functionalization was done by using the hydrosilylation method with no cross-linker. The sequence of all the steps used for the detection of the binding process is as follows:

- The first step is to functionalize the SiNW by hydrosilylation method as explained in the earlier section and then immobilize the primary antibody which is covalently bonded to the –alkyne terminated surface of the SiNW by click-chemistry.
- The next step is to set the baseline resistance by taking measurement with the Phosphate Buffered Solution (PBS) on the SiNW.
- Increasing concentrations of the secondary antibody (400 ng/ml, 4μg/ml and 40μg/ml) are then immobilized on the surface of the SiNW and electrical measurements are recorded for 20 seconds, which gives 20 recording points of the resistance values on each of the four SiNW on the chip.

SiNW surface is washed with PBS between all steps to remove any non-specific bound antibody. Figure 7.3 shows the schematic diagram of the detection principle of primary to secondary antibody system on SiNW using first technique.

7.2.1.1 Measurement Results

All the electrical measurements were done by using the setup for 1st generation with Labview interface explained in chapter 5 and are represented in figure 7.4.

7.2.1.2 Discussion

This experiment was performed in the first year of the research project when the first prototype of the SiNW Bio-FET using in-situ doped polysilicon was made by

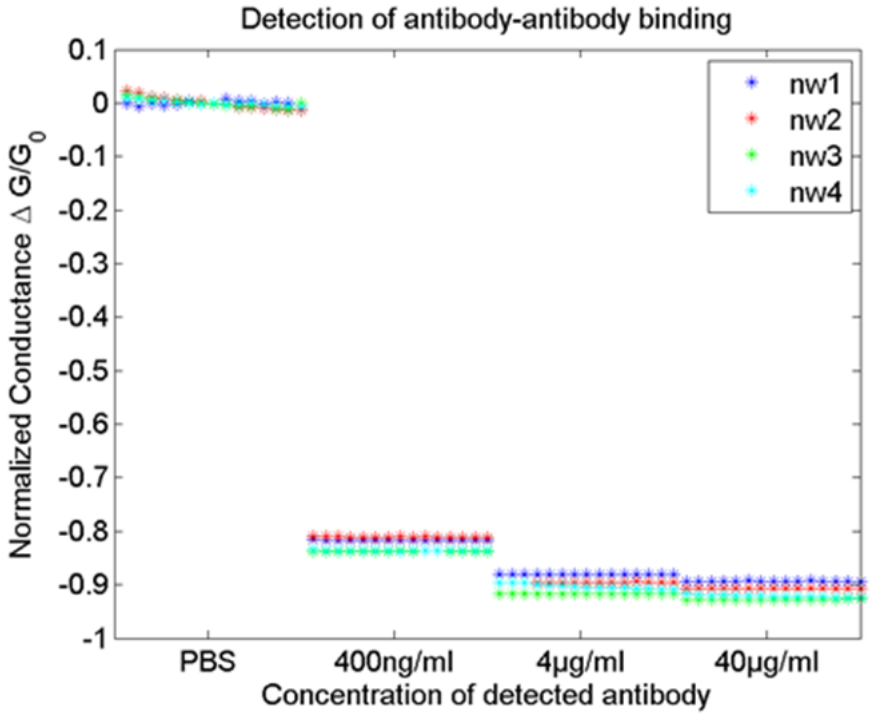


Figure 7.4: Change in conductance upon binding of different concentrations of the secondary antibody to the SiNW Bio-FET surface functionalized with the primary antibody. Here nw1-nw4 represents SiNW1-SiNW4 present in one chip (Phd summer school teaching results)

1st generation process, where the microfluidic channel was made in SU-8. The background behind the development of this prototype is explained in detail in chapter 8. From the plot it can be seen that all the four SiNWs responded in the same way when the different concentrations of the secondary antibody are added which bind specifically to the primary antibody. The change in the conductance after addition of increasing concentrations of secondary antibody is seen due to the attachment of the more secondary antibodies to the unbounded primary antibody immobilized on SiNW. However, the conductance change between 4μg/ml and 40μg/ml of secondary antibody is comparatively low that can be attributed to low number of available binding sites (assay saturation). This change in response of the SiNW upon binding of analyte proves that the in-situ doped polysilicon can be used for detection of biomolecules.

But at the same time, several problems were identified during the measurements. The first problem was observed when the impedance of the SiNWs started to get a phase shift during the detection steps. This could be due to current leaking from the SiNW into the liquid caused by the bad insulation of native oxide of the SiNW or could be due to etching of SiNW during the functionalization process that happens when the gold in the side gate electrode leads to the galvanic reaction in the presence of HF as explained in chapter 6.

The second problem observed was that out of three devices only one device showed the behavior that was according to the expected binding of the analyte to SiNW Bio-FET surface. This could be due to improper functionalization of the SiNW surface that might have resulted in malfunctioning of the device.

The third problem that was observed during the experiments was the delamination of the SU-8 microfluidic channel at different stages of functionalization. The possible reason after discussion in the group and talking to expert users was found to be that the humidity level in the cleanroom may have gone high during the SU-8 process which may cause possible delamination.

Based on these findings, the changes in the fabrication process were made by removing the side gate electrode and by making a process where polyimide could be used as microfluidic channel. At the same time, the investigation into the surface coverage after functionalization was started by PhD student Andrea Pfreundt.

7.2.2 DNA hybdridization sensing

This model system was chosen due to the high amount of negative charges in the DNA backbone that can easily change the current flow in SiNW due to its field effect upon binding. The functionalization method used for this sensing experiment was silanization method. The sequence of steps followed for sensing of DNA hybridization is as follow:

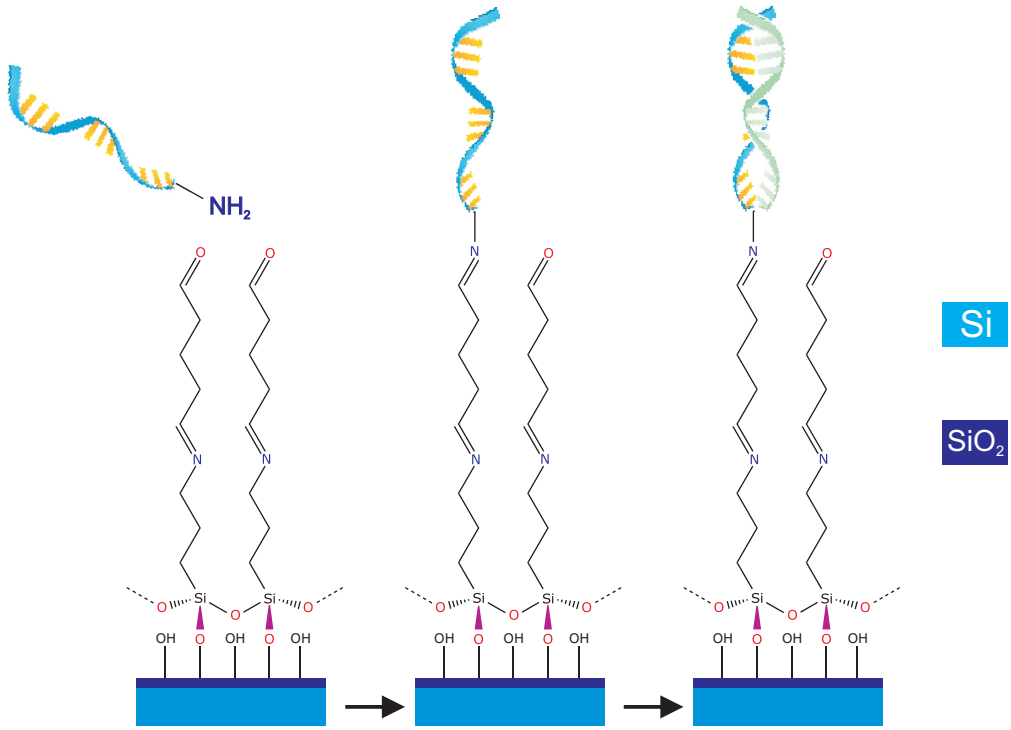


Figure 7.5: DNA Hybridization sensing sequence on functionalized SiNW surface where amino conjugated ssDNA is immobilized on the SiNW surface (via Glutaraldehyde) followed by specific binding of the complementary DNA

- Monolayer formation of APTES on the SiNW.
- Addition of Glutaraldehyde as a cross-linker to the APTES layer.
- Immobilization of the amino conjugated single-stranded DNA (ssDNA) that can bind specifically to the carboxylic part of the Glutaraldehyde linker.

- A negative control is also performed to verify the correct response of the SiNW. This is done by immobilizing non-complementary DNA (ncDNA) on the surface.

- The positive control is then made by immobilizing the complementary DNA (cDNA) on to the surface which should bind specifically to the ssDNA.

The resistance of the SiNW was recorded after each step by continuous measurement for duration of around 30 seconds which results in 30 recording points at each step. Washing with Phosphate Buffered Solution (PBS) is done after each step to get rid of non-specifically bound molecules that will affect the signal of the SiNW. Figure 7.5 shows the schematic diagram of the steps involved in DNA hybridization sensing

7.2.2.1 Measurement Results

The successful measurements were made on sensing DNA hybridization using SiNW Bio-FET devices. Figure 7.6 shows the measurements made on SiNW after each step of detection.

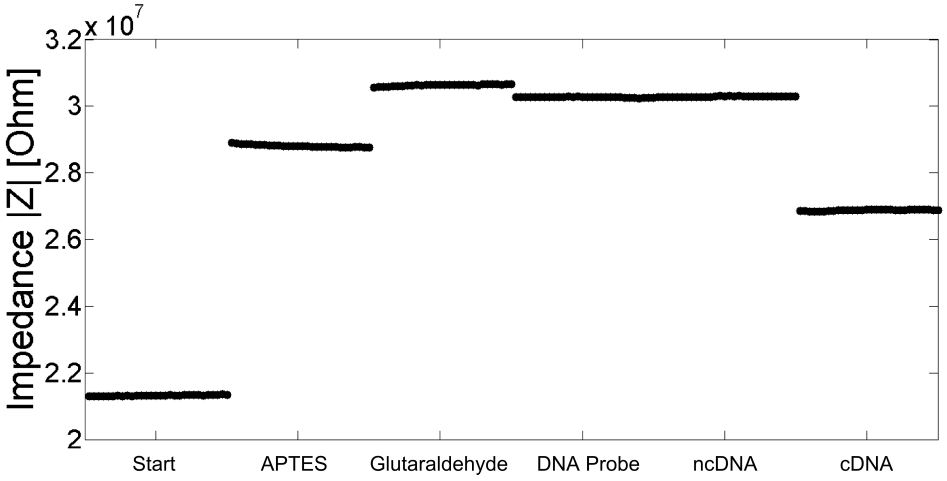


Figure 7.6: Measurements of SiNW resistance after each step of DNA hybridization sensing (courtesy Dorota Kwasny)

The sequence of resistance measurements made after each step is as follow:

- The resistance of the SiNW was measured before starting the experiment that was considered as baseline value.

- After APTES layer the resistance of the SiNW increased due to positive gate potential formed on top of SiNW.

- The addition of Glutaraldehyde increased the resistance further due to increase in positive charge carriers.

- The resistance then decreased after immobilization of single stranded DNA on the SiNW surface due to negatively charged carriers in DNA.

- The resistance of the SiNW remained unchanged when the non-complementary DNA was immobilized on the SiNW surface. This is the indication that no binding occurred on top of SiNW and thus no change in potential was detected by the SiNW.
- The resistance of the SiNW dropped when the complementary DNA was immobilized on the SiNW surface indicative of the binding event that occurred when complementary DNA came together with ssDNA resulting in accumulation of negative charge carriers on top of SiNW and subsequent decrease in the resistance of SiNW.

7.2.2.2 Discussion

The above experiments were performed on the Bio-FET devices made from 1st generation process when the SU-8 was replaced by polyimide. The polyimide in this experiment was formed using Si_3N_4 as masking material. From the above results, it was proven that the SiNW is sensitive enough to detect DNA hybridization process. However, they were not reproducible when the sensing experiment was repeated. The initial reasons were thought to be poor sensitivity of SiNW or improper functionalization of SiNW.

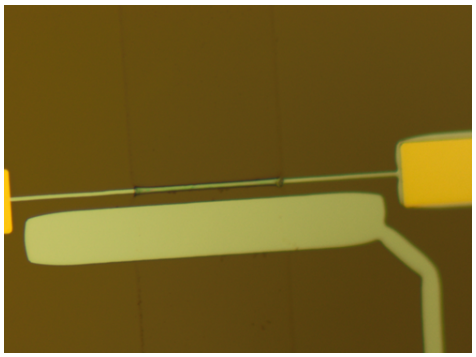


Figure 7.7: Microscope image showing SU-8 layer on top of SiNW after cleaving SU-8 microfluidic channel from the SiNW chip (courtesy of Andrea Pfreundt)

Detailed investigations were made later by Andrea Pfreundt on the reproducibility of the functionalized layer which showed that the protocol was not producing stable monolayers every time. This protocol was then replaced by the protocol made by Karen Martinez research group in University of Copenhagen. At the same time steps were taken to improve the sensitivity of SiNW so that the measurements could be made in the sub-threshold regime of Bio-FET device, based on the findings by Lieber[72]. In the 1st generation process devices the sub-threshold regime was not achieved due to certain factors that are discussed earlier in chapter 6.

Another factor that was hurdle in reproducing the DNA sensing results was the polyimide process. This first experiment was performed on a chip passivated by polyimide patterned by Si_3N_4 mask but later on, findings during PI process optimization forced to shift to use Al mask to pattern PI in order to standardize the process for all heights of microfluidic channels. But this shift also brought some problems with it in the fabrication results. The recipe to etch the PI was not good as it was producing residue layers discussed in chapter 4. This residue layer was also influencing in the bad functionalization of the SiNW.

While the optimization of process recipe for PI was in progress, a shift was made back to an SU-8 microfluidic channel by monitoring the humidity level to avoid any delamination. But after the fabrication, the DNA sensing failed on 2nd generation process chips, where the reason was found to be that a small amount of SU-8 was covering the SiNW which resulted in bad functionalization, hence no sensing. Figure 7.7 shows the image of the SiNW after removing the SU-8 microfluidic channel. It is clear from the image that some SU-8 is covering the SiNW, despite the fact that the SU8 process had been optimized. It was concluded that SU-8 microfluidic channels are not good for SiNW biosensors, considering the significant optimization work required to build them.

7.2.3 Primary to secondary antibody binding detection

The second attempt was made to detect primary-secondary -antibody binding where the sensing experiment was carried by using –H terminated Si surface and utilizing EDC/NHS cross-linker while avoiding click chemistry. The functionalization steps used for the detection of the binding process are as follows:

- Native oxide was removed with HF
- The 10-N-Boc-amino-dec-1-ene was immobilized on the SiNW and was left under lamp over night
- The Boc part was then removed by boiling the chips
- EDC-NHS and the primary antibody were then added together
- Increasing concentrations of secondary antibody was then immobilized (with an incubation time of around 5 mins each) that would attach to the primary one thereby changing the conductance of the SiNW.

Figure 7.8 shows the schematic diagram of all the steps involved in the detection of the two-antibody system.

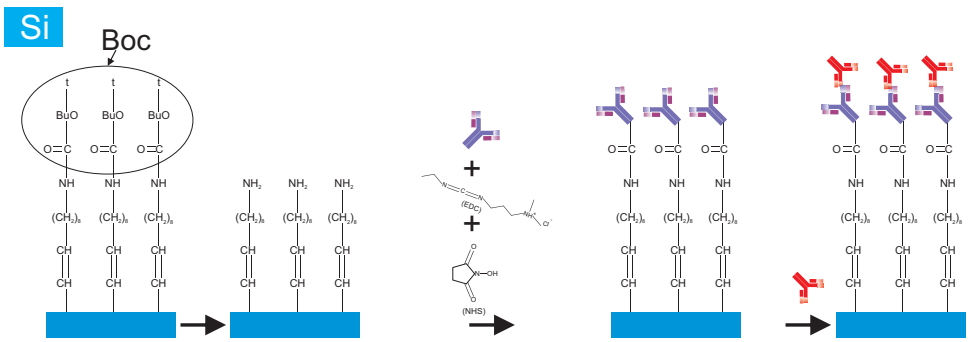


Figure 7.8: Schematic diagram of all the steps of detection of secondary antibody by utilizing –H terminated Si surface to functionalize the SiNW with primary antibody

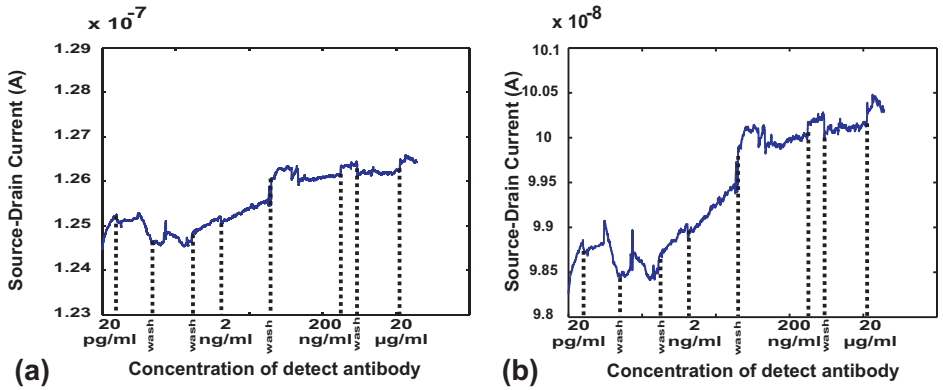


Figure 7.9: Real time detection results of different concentrations of the secondary antibody immobilized on the functionalized Bio-FET device.(a) 1st NW on the chip (b) 2nd NW on the chip (courtesy Pfreundt and Zarmeena)

7.2.3.1 Measurement Results

The CMOS measurement setup was used to make real time measurement of the binding event. Figure 7.9 shows the real time sensing results from the above mentioned functionalization protocol.

For a negative control, another chip was used where no functionalization steps were performed. Figure 7.10 shows the real time measurement made on the negative control chip.

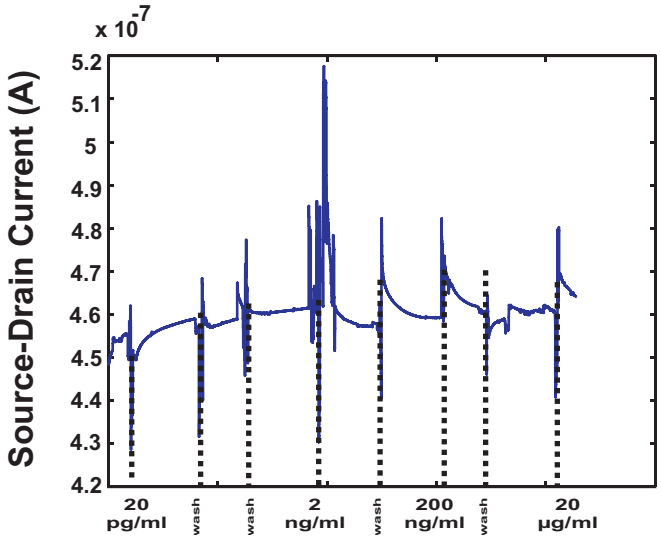


Figure 7.10: Real time measurements on negative control Bio-FET device with no functionalization at different concentration of secondary antibody immobilization

7.2.3.2 Discussion

The above experiment was conducted on the Bio-FET devices made by using 1st generation process where PI was patterned by Si_3N_4 mask, and the SiNWs of the test chip were fully functionalized while for the negative control no functionalization was performed. Unfortunately, two SiNWs on the test chip were damaged which didn't allow measurements on them.

The change in the source-drain current of SiNW upon immobilization of different concentrations of secondary antibody on both the test chips is quite clear while no change was observed in the negative control chip. However, the recorded signal was extremely unstable, showed drift and there doesn't seem to be any direct relation between the concentration and the change in current. Both working nanowires on the chip show precisely the same behavior though, which could mean that part of the observed drift can be due to the measurement setup. This experiment also produced some promising results but due to poor reproducibility in the functionalization of the SiNW surface further experimentation was stopped.

One of the factors influencing the functionalization was improper removal of Boc-part in the first step while boiling the chips. Further experimentation was stopped until the improvement of the functionalization protocol.

7.3 Bio-sensing with 2nd generation process devices

After the slight improvement in the sensitivity of the SiNW in the 2nd generation process as explained in chapter 6, the detection of the Natural Killer Group 2D (NKG2D) cancer biomarker was tested in collaboration with one of the EU project partners at University of Copenhagen, as part of the milestones set in the project.

NKG2D is an activating receptor that is expressed on immune cells and is implicated in various infections and cancers. NKG2D ligands are over-expressed in various types of tumor tissues and ULBP2 is one of these. This sensing experiment was carried out by silanization method where the APTES functionalization was done with the new protocol developed at University of Copenhagen. The sequence of the steps for the NKG2D detection is as follows:

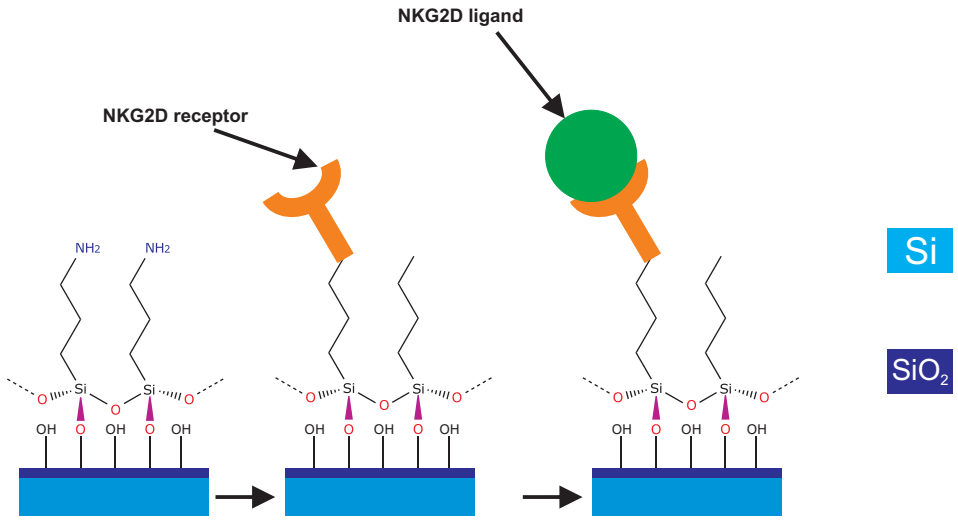


Figure 7.11: Schematic diagram of all the steps of detection of NKG2D by functionalization of the SiNW surface with NKG2D receptors

- APTES monolayer formation by silanization method as explained earlier.
- Immobilization of NKG2D receptor to the APTES
- Base line of the SiNW impedance measurement is done with PBS

- Adding RPMI medium without any cells
- Adding supernatant from cancer cultured cells which contains the NKG2D ligand secretions.
- Adding supernatant from the cancer cultured cells treated with the compound that increases the secretion of the NKG2D ligands.
- Repeating the above sequence for one more time
- Adding pure NKG2D ligand (ULBP2) attached with Fc tag that is bought from the supplier

5 mins of incubation time is given on each step while making the real time measurement of the binding process by using CMOS setup. Figure 7.11 shows the schematic of the detection principle for NKG2D ligands.

7.3.1 Measurement Results

The first change in the signal is detected at step 2 label in the figure 7.12 when the RPMI medium (without cells) is added on the chip. All the SiNW responded in the same way. The second change is observed at step 3 by the addition of culture supernatant from cancer cells with low NKG2D concentration. Thereafter, relatively

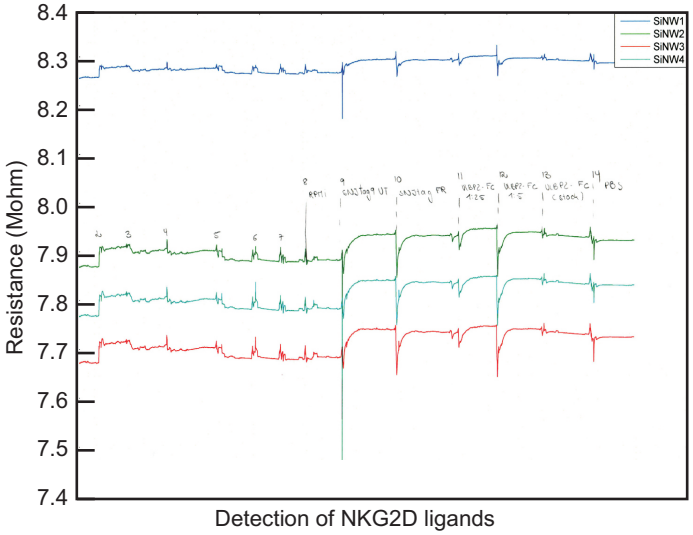


Figure 7.12: Real time measurements results of NKG2D ligand binding to receptor using SiNW Bio-FET

high concentration of NKG2D from treated cells has changed the signal at step 4. This sequence is repeated again from step 5 to 7 and continuous drop in the resistance of the SiNW is observed due to binding of additional molecules. At step 8 RPMI is added which keeps the signal unchanged. From step 9 to 14 the pure and highly concentrated NKG2D ligands modified with an Fc tag are added. This changes the signal but surprisingly in the opposite direction than before. That could be due to the fact that differences in the constitution of RPMI medium used for cultured cells and 1% Bovine serum albumin (BSA) in PBS used for preparing lyophilized NKG2D ligand.

7.3.2 Discussion

This experiment was done as a first trial to see if the SiNW produced by 2nd generation process could respond to the immobilization of NKG2D. The results were promising but also shows that the nanowires are not very sensitive, which is expected considering that the 2nd generation chips could not be fully depleted. This experiment has not repeated with 3rd generation device due to shortage of time but is currently underway.

7.4 pH Sensing

After the fabrication by 3rd generation process the first test to check the sensitivity Bio-FET devices was done by making pH measurements. The experimental setup used for this test is shown in the figure 7.13. The measurements were made by

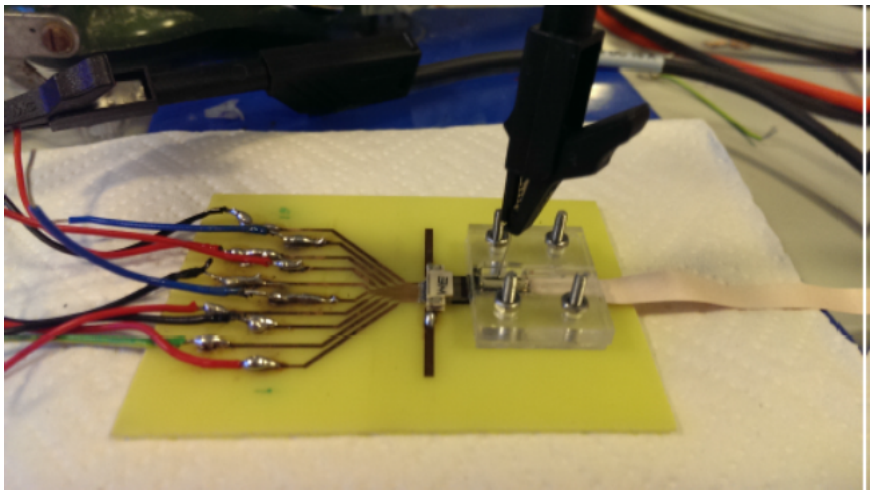


Figure 7.13: Measurement setup used for pH sensing experiment. The liquid gate is applied from the top by using holder with crocodile pin to hold the platinum wire

first pipetting the pH solution on top of the chip and then the back gate was set to constant potential of 0 V while the source-drain voltage (V_{DS}) was swept from -1 V to +1V with the step of 0.1 V. Six pH buffered solutions were prepared (pH 1.73, 2.98, 4, 7, 10 and 13 as measured by the pH meter) and were used for the pH sensing experiment. The sequence of the measurement was dry, MilliQ water, pH7 solution, pH1.73 solution, pH7 solution, pH 2.98 solution, pH7 solution, pH4 solution, pH7 solution, pH10 solution, pH 7 solution, pH13 solution and pH7 solution. The chip was washed three times with MilliQ and dried by compressed air after each measurement. Figure 7.14 shows the measurements results From the results it can be seen that at lower pH values the difference measured by SiNW is comparatively small while at pH 13 the SiNW showed a significant change followed by the same change in pH 7 measurements made soon after pH13. This is due to the fact that pH13 is a basic solution that attacks the SiNW and etches it which leads to the change in the signal for different dimension of SiNW which was verified by the pH7 measurement made after pH13. To troubleshoot this behavior, the test was made on the leakage of current from SiNW into solution as the above behavior was seemed to be due to current flowing through liquid which has less resistance compared to the SiNW.

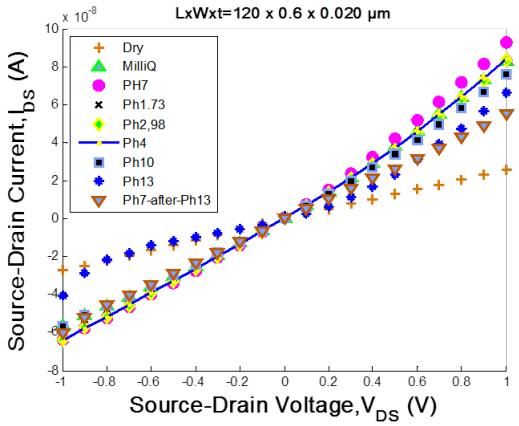


Figure 7.14: pH sensing results showing the source-drain current I_{DS} vs source drain voltage V_{DS} curve when the V_G was set to 0V.

For this purpose, the liquid gate was used by dipping the platinum wire into the solution with pH 7. The source-drain potential was set to 300 mV while liquid gate was swept from -1V to +1V with the step of 0.1 V. Figure 7.15 shows the behavior of the SiNW and the leakage current. From this plot it is clear that the native oxide

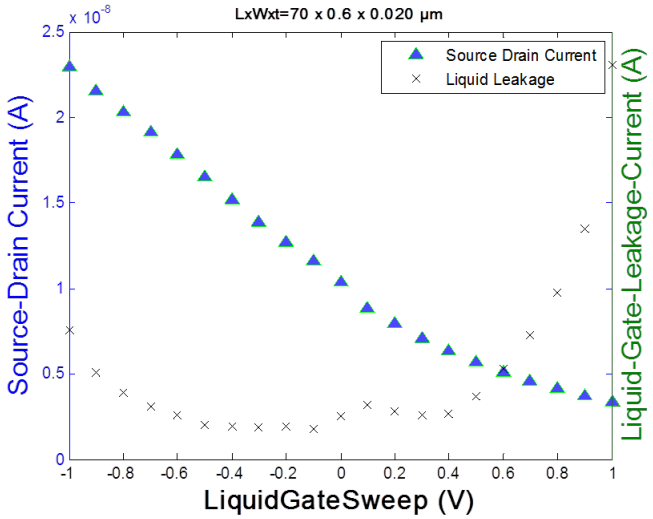


Figure 7.15: I_{DS} -vs V_{LG} plot showing the response of SiNW by changing the liquid gate potential along with the leakage current.

is not completely isolating the SiNW and the percentage of leakage current is high in the liquid which is influencing the pH measurements as well. The leakage is not symmetric, as would have been expected. This could have something to do with the way the measurements are performed, as we first sweep the voltage from 0 to -1 V to 1 V and back to 0. It is possible that damage occurs to the native oxide at the high negative voltage, leading to a higher leakage on the positive side. Native oxide is known for its not so good isolating properties. To overcome this problem, an extra fabrication process step is added into the 3rd generation process, where the isolation of SiNW is done soon after patterning by depositing 5 nm of Atomic Layer Deposition (ALD) of Al_2O_3. The other choice was doing dry oxidation at 900℃ for 5 mins to grow 5 nm of SiO_2 but there was risk of losing more dopants. The

fabrication of the Bio-FET devices is completed at this point but the measurements will be done in the near future.

Chapter 8

Alternative Fabrication Processes

This project was a continuation of the master's thesis written by Michael Jørgensen, where a fabrication process for the SiNW was developed by using the ion-implantation method to highly dope source-drain contacts on single crystal SOI wafer, while keeping the SiNW to a relatively low doping level. The process developed by the student was used as the starting point for fabrication of Bio-FET devices. Figure 8.1 shows the schematic diagram of the fabrication steps using SOI wafer.

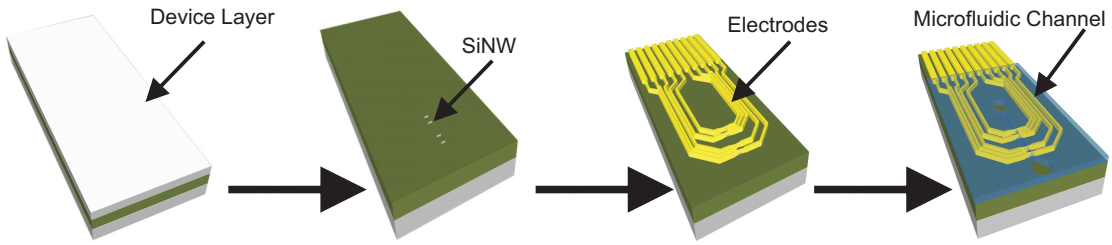


Figure 8.1: Schematic diagram showing step by step fabrication of the SiNW device(a) SOI substrate(b)Pattern SiNW by dry etching and ion-implantation of source-drain (c)e-beam evaporation of Au and lift-off process(d)Microfluidic channel formed using SU-8

This process was followed also in the beginning of the project in order to reproduce the results obtained by the master project. The SOI wafers that were used were very expensive and therefore we had a limited amount of wafers available for doing this process, which is one of the reasons it was eventually abandoned.

8.1 Fabrication Steps by ion-implantation method

The first batch of SiNW Bio-FET devices was made by using the above mentioned fabrication process. All the fabrication steps along with the problems experienced are explained in detail below.

8.1.1 SOI Wafer selection

SOI wafers with the specifications shown in table 8.1 were ordered from "University Wafer" for this process whereby each wafer costed around $325, compared to the

$10 that a standard wafer costs.

Type/Dopant	Orientation	Device Layer Thickness(μm)	Resistance(Ω-cm)	Oxide Layer(μm)	Wafer thickness
P/B	<100>	0.05+/-0.002	1–20	0.404+/-0.002	525+/–20

Table 8.1: Specifications of the SOI wafers

8.1.2 Wafer Thinning

To fit the devices in the ZIF socket the thickness of the wafers has to be reduced from 525μm to 350μm. For this purpose the wafer was thinned down as a first step from the backside by Deep Reactive Ion Etching (DRIE) process. The recipe used for this process can be found in the appendix

8.1.3 Patterning Silicon Nanowires

As a second step, the SiNW were patterned by Reactive Ion etching (RIE) using photoresist as a mask. The mask contained structures of SiNW without contact pads as shown in figure 8.1b. A mixture of SF_6 and O_2 was used for etching the silicon and by using the "End Point" detection function in the machine the optimum etching time was established.

8.1.4 Ion-Implantation of source-drain

The next step was to ion-implant the source-drain with boron dopants. For this purpose, the pattern of contact pads was made in photoresist by photolithography which was used as masking material for ion-implanting source-drain in SiNW. The parameters used for ion-implantation are shown in table 8.1

Dopant	Orientation	Dose (cm^2)	Energy (KeV)	Masking	Current(μA)
Boron	<1-0-0>	$5e^{14}$	15	Resist	< 100

Table 8.2: Ion-Implantation parameters

8.1.5 Metallization

The source and drain were metallized by e-beam evaporation of 20 nm Cr and 100 nm Au and a lift-off process. To check the connections and measure the resistance across the SiNW, two probe measurements were done.

8.1.6 Microfluidic channel

As a last step SU-8 polymer, which is a photosensitive epoxy resin with the thickness of around 70μm, was patterned as microfluidic channel on top of the SiNW chip. The recipe used to make these SU-8 channels is included in the appendix.

8.2 Device Testing after ion-implantation

The first tests on the devices failed due to loss of connection between the source and the drain. The investigations made to diagnose the problem are stated as follows:

8.2.1 Metallization Problem

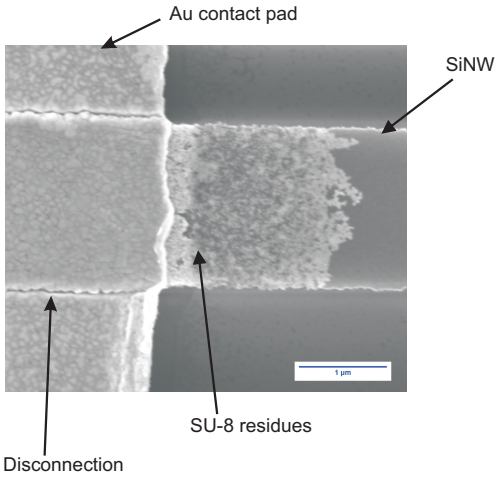


Figure 8.2: Scanning Electron Microscopy image showing the disconnection between Au and SiNW

The first step taken to diagnose the problem was removal of the SU-8 polymer from the chip by leaving it overnight in a Dimethyl-Sulfo-oxide (DMSO) solution and investigating the coverage of Au over the SiNW under a Scanning Electron Microscope (SEM). Upon inspection through SEM it was found that the Au contacts were not uniformly covering the SiNW, which led to the problem of lost connection. Figure 8.2 shows a SEM image where the disconnection between Au and SiNW is clearly visible when the SU-8 is removed from the chip. This problem was fixed by making changes in the SiNW patterning mask by combining the contact pads with SiNW so that metal is deposited on top of Si. SEM image 8.3 shows the better connection of Au and SiNW after improvement.

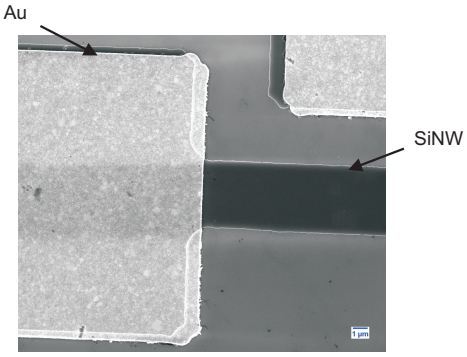


Figure 8.3: Scanning Electron Microscopy image of Au better coverage on SiNW with a slight mis-alignment

8.2.2 Ion-Implantation Parameter

In the second batch of ion-implantation, despite improvement of connection between Au and SiNW, there was still no connection between source and drain. The troubleshooting was then carried out on each of the fabrication process steps. Upon investigation of the ion-implantation parameters by running a SRIM simulation, it was found that the energy of 15 keV for ion implantation was not appropriate for a 50 nm thick device layer on a SOI wafer. The optimized energy parameters for ion-implantation were then calculated using SRIM simulations. Figure 8.4 shows the image of the results by SRIM simulation, where the dopants distribution before and after optimization are stated. The peaks in the graphs show the peak concentration of dopants within the target depth of Si.

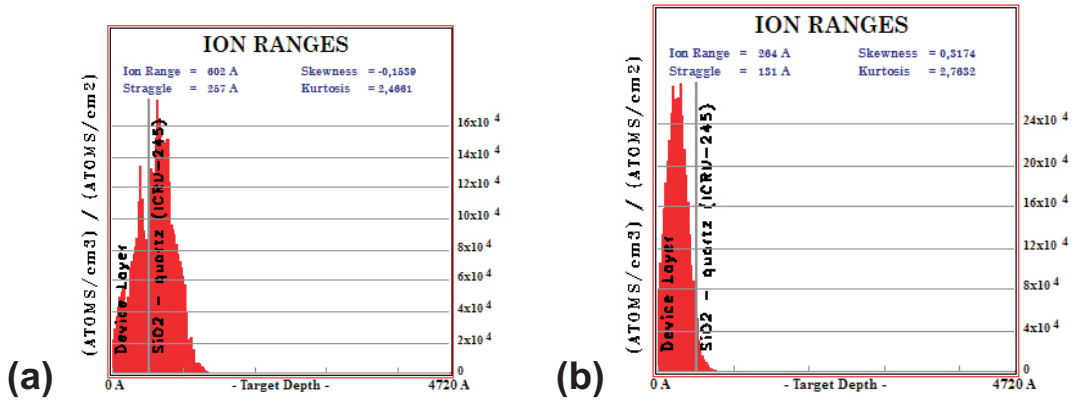


Figure 8.4: SRIM simulation results for dopant distribution over the depth of Si after ion-implantation (a) When energy is set to 15 keV (b) When energy is set to 6 keV.

From the above figure it is quite clear that 15 keV was implanting boron atoms in the buried oxide instead of the device layer, whereas 6 keV is the right energy parameter to be used for ion-implanting the contact pads.

However, after discussions with the ion-implantation facility, 6 keV was deemed to be a very low level of energy to ion-implant the boron target. Diflouroboryl (BF_2) with the energy of 26 keV was recommended by them as a better option that can provide the same doping concentration level on 50 nm thick Si. Therefore the suggested parameters were chosen to ion-implant the device layer of SOI wafer.

8.2.3 Annealing Parameters

As part of further rectification of the process sequence, a literature review was also done on dopant activation parameters. It was found that rapid thermal annealing (RTA) is a better alternative to the conventional thermal annealing in the furnace [107, 108, 109]. The annealing conditions to activate dopants were also optimized by using the RTA machine. To avoid wasting the expensive SOI wafers in optimizing the annealing conditions, few wafers with the same specifications were made from undoped polysilicon that were also implanted with BF_2. Different annealing conditions were then defined by keeping the ramp up and ramp down time to 120 seconds while changing the temperature and its duration to get uniform distribution of dopants in source-drain contacts. To examine the distribution of boron within

silicon, SIMS measurements were made on each sample.Figure 8.5 shows different annealing conditions that were used to activate the dopants along with the respective SIMS measurements. Sheet resistance measurements were also made on the

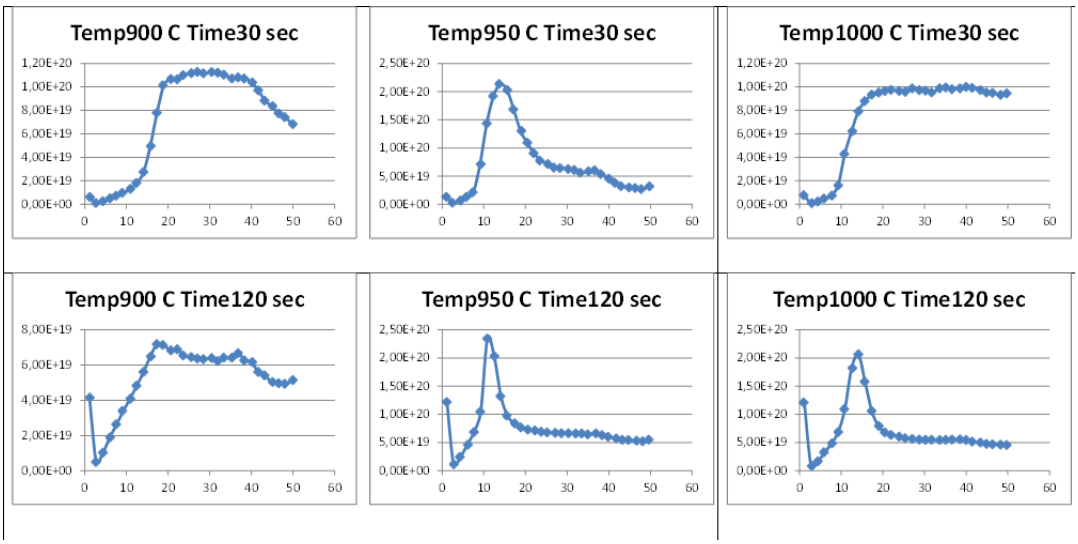


Figure 8.5: Annealing conditions used in RTA along with the SIMS measurements results

above mentioned samples by the four probe measurements (done by the company CAPRES using their micro-probes). Table 8.3 shows the sheet resistance values on each annealing conditions.

Annealing conditions	Temp 900℃ Time 30 sec	Temp 950℃ Time 30 sec	Temp 1000℃ Time 30 sec
Sheet resistance (Ω)	1745	Not possible	1352
Annealing conditions	Temp 900℃ Time 120 sec	Time 950℃ Time 120 sec	Temp 1000℃ Time 120 sec
Sheet resistance (Ω)	1817	Not possible	1536

Table 8.3: Sheet resistance measurements on annealed samples

Based on the above measurements, the best annealing condition selected was 1000℃ for 30 secs. Using 1352 Ω as sheet resistance (R_S), thickness of device layer (5.3×10^{-6}cm) the resistivity ρ was calculated by using the formula

$$\rho = R_S.d \tag{8.1}$$

This gives the value of ρ as

$$\rho = 7.95 \times 10^{(} - 3)\Omega \tag{8.2}$$

By looking into the resistivity vs impurity concentration chart from [66] the dopant concentration is around $3 \times 10^{20} atoms/cm^3$ as shown in figure 8.6. This parameter was then used to first fabricate the polysilicon SiNW before using it on SOI wafers.

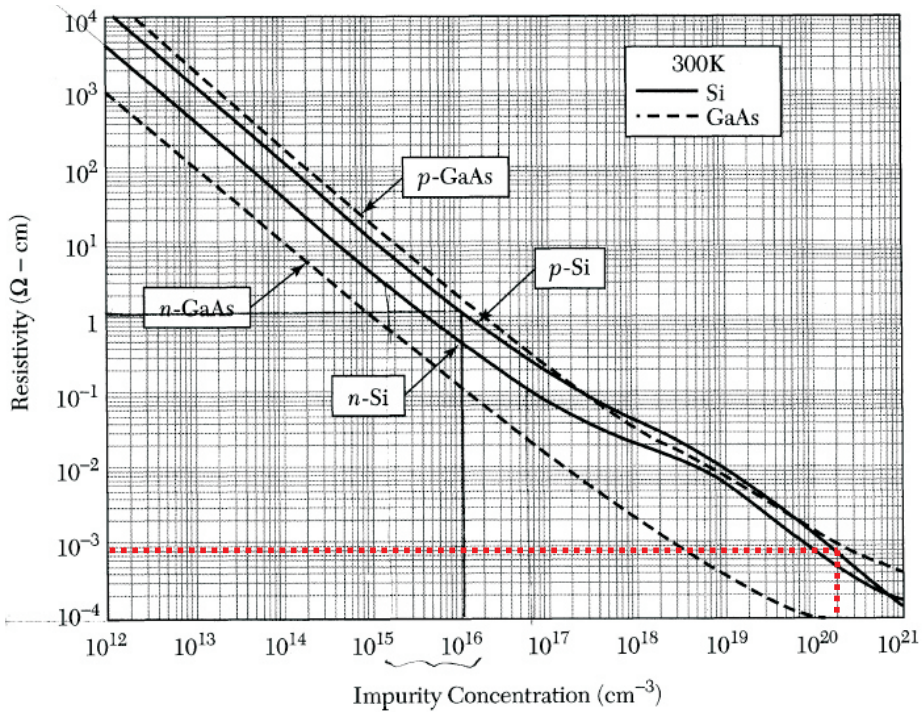


Figure 8.6: Resistivity vs impurity concentration chart from [66] showing the achieved dopant concentration after RTA at 1000℃ for 30 secs

The fabrication of polysilicon SiNW wafer faced problems in the RTA step due to problem in the heating lamp and cooling water in the machine. A lot of damage occurred to the structures on the wafer at this step due to which this process was halted until the machine got fixed.

8.2.4 Conclusion

Since this project was a part of an EU Marie Curie program, the main constraint was achieving the milestones set in the project on time. The first milestone was to make SiNW Bio-FET devices within the first year and make measurements on cancer biomarkers supplied by the EU partners. The other constraint that came up early in the project was unavailability of 4 inch SOI wafers with the same specification that were used to optimize the fabrication process. To overcome these constraints and to reduce the reliance on expensive and difficult to get SOI wafers it was decided to leave this process at this stage and to make a process that is cheap, robust and easy to make at DTU cleanroom facility.

The two options available as an alternative to the ion-implantation methods were:

- Diffusion method
- In-situ doped polysilicon method

The work on developing the fabrication process for both the methods was started simultaneously but due to a stack of problems occurring in both the methods, the in-situ doped polysilicon method was prioritized due to its potential of producing faster, cheaper and reproducible devices. The optimization of the whole fabrication

process by using in-situ doped polysilicon is explained earlier in this thesis. In the next section, the process developed for diffusion method is explained.

8.3 Fabrication of SiNW by Diffusion method

In this method, boron rich glass known as Boron Silicate Glass (BSG) was deposited by PECVD technique and patterned on top of the silicon source and drain contacts of a future SiNW by a wet etching method. The dopants were then diffused into these contacts by RTA.

8.3.1 Fabrication process steps

Polysilicon based SOI wafers with 170 nm buried oxide and 50 nm undoped polysilicon device layers were used to develop fabrication process for SiNW by diffusion process. The complete process is shown in figure 8.7. Following are the process steps that are different from ion-implantation method:

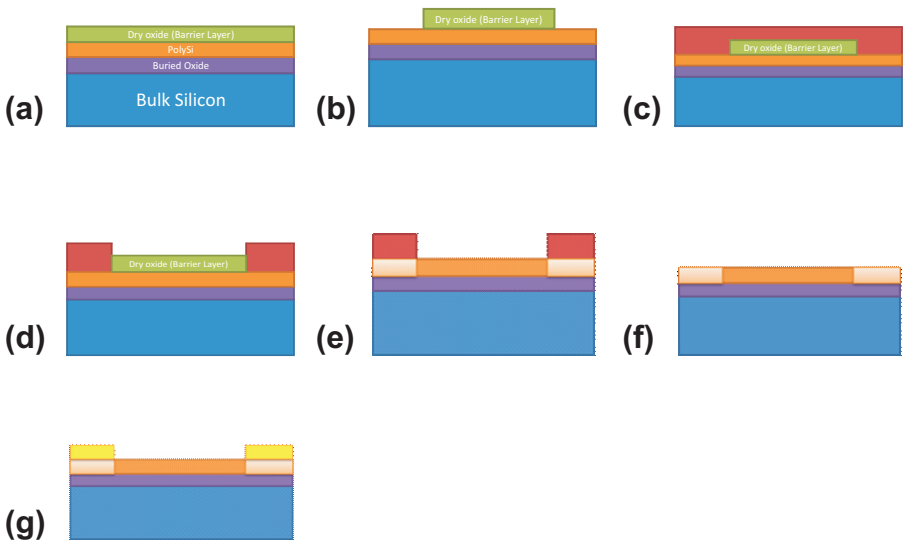


Figure 8.7: Schematic diagram of all the fabrication steps for diffusion process. (a) Deposition of buried oxide as barrier layer on top of polysilicon (b) Patterning of barrier layer to protect the places from doping (c) Deposition of BSG all over the wafer by PECVD (d) Patterning of BSG on top of places to be doped (e) Remove barrier layer and RTA of the sample (f) Remove BSG (g) E-beam evaporation of Cr/Au

8.3.1.1 Deposition of Barrier Layer

The first step is to pattern SiNW by RIE process followed by the deposition of the diffusion barrier layer on top. 200 nm thick tetraethoxysilane (TEOS) based SiO_2 is deposited in the TEOS furnace. The barrier layer is then patterned to protect the parts of the wafer that should not be doped. This is done by using patterned photoresist as a mask and BHF etching to remove TEOS oxide.

8.3.1.2 Deposition of Boron Silicate Glass (BSG)

The second step is to deposit 400 nm of BSG on top of the wafer using PECVD technique. Before this, the recipe of the BSG was optimized in PECVD machine, where the gas flow of B_2H_6 and SiH_4 were adjusted in an optimum ratio to get the boron rich glass layer. The testing of the BSG to confirm boron content in the glass was done by wet etch removal of BSG in BHF. The high amount of boron in the BSG glass reduces the etch rate of the glass significantly. The recipe made for this process gave an etch rate of BSG of around 15 nm/min vs the 100 nm/min for standard glass [101]. After the deposition the BSG is also patterned by protecting the contact pads with the photoresist pattern of the silicon nanowire contacts and etch away BSG.

8.3.1.3 Diffusion of dopants

The next step is to diffuse down the dopants into the source and drain of SiNW. For this purpose, RTA technique was used, where different annealing conditions were tested. Quick tests were made by using two probe measurements after each annealing test. Table 8.4 shows the parameters used for RTA and the two probe measurements Based on these results, the parameters chosen for diffusion process were 10 seconds

Ramp up time	Annealing Time	Ramp down time	Temperature	TWO PROBE
120 sec	1 sec	120 sec	1000℃	$1.2(K\Omega)$
120 sec	10 sec	120 sec	1000℃	$0.24(K\Omega)$
120 sec	60 sec	120 sec	1000℃	$0.4(K\Omega)$
120 sec	10 sec	120 sec	900℃	$0.203\ (K\Omega)$
120 sec	10 sec	120 sec	800℃	(Ω)
120 sec	20 sec	120 sec	700℃	$61.34\ (K\Omega)$

Table 8.4: RTA conditions and two probe measurements

annealing at 1000℃. These parameters were used to first test on the wafer without any pattern and measure the sheet resistance after diffusion process. The sheet resistance by four probe measurements on the sample was found to be $2.4 \times 10^{-3}\Omega$-cm. This value of sheet resistance gave the required dopant concentration of around $5 \times 10^{19} atoms/cm^3$ by referring to the figure 8.6

The results show a certain dependence of the two probe measurements with annealing time and temperature.

8.3.1.4 BSG and Barrier Removal

Both the BSG and barrier layers are removed by BHF etch while protecting the other parts of the wafer as shown in figure 8.7

8.3.2 Conclusion

During the development of this process, the shift to the Si_3N_4 buried insulator was made in 2nd generation process of in-situ doped polysilicon to obtain the SiNW with less width. This change was also made in the diffusion process but since the Si_3N_4

layer was giving leakage problems at high temperature it got even worse for diffusion process because the high ramp up time to reach 1000℃ and high ramp down time was creating problems in the insulation behavior of the nitride layer. This process was also set on hold until the solution was found for the good insulation properties of the nitride layer.

Chapter 9

Conclusion and Outlook

The aim of this research project has been to develop a low cost, robust fabrication process for SiNW Bio-FET sensor with high yield and reproducibility while keeping the sensitivity of the biosensor to an optimal level. To integrate the biosensor with microfluidics system that can further be developed into POC device which can be operated with smart phones which requires low level of power consumption.

To achieve these goals three generations of fabrication processes has been developed to investigate a novel in-situ doped polysilicon material as a possible candidate for SiNW Bio-FET sensor in a junctionless transistor configuration. First fabrication process involved dry etching process to pattern SiNW after photolithography to achieve SiNW with lowest feature size in microns. These devices with 50 nm thick SiNW and doping concentration of around $3 \times 10^18 atoms/cm^3$ showed the FET behavior upon electrical characterization by using back gate voltage to change the source drain current in the SiNW but the sensitivity was measured to be at low level since the complete depletion of the SiNW was not achieved. These devices were used for bio sensing experiments as well where DNA hybridization and two antibody systems experiments were successfully tested. However, the results were not reproduced due to possible malfunctioning of the functionalization protocol and low response level in SiNW.

The fabrication process was improved in the second generation process by replacing the dry etching with wet etching process to pattern SiNW after photolithography to achieve SiNW with lowest feature size in nanometers and by replacing 170 nm buried oxide with 50 nm buried nitride. To improve the sensitivity of the SiNW annealing of the polysilicon was done at 900℃ for 30 mins to change the grain size and activate the dopants in the SiNW, and the thickness was reduced to 30 nm. These devices were tested by electrical characterization and again low sensitivity was measured as the complete depletion was still not possible even by applying high back gate voltage. The possible reasons were then identified as no change in grain size and increase in dopant concentration due to furnace recipe execution sequence. These devices were also used for sensing NKG2D biomarker where the response of the SiNW was not significant. The possible reason was found that baseline for the experiment was not the same throughout the experiment and the response of the SiNW was not high enough.

In the third generation process, the discrepancies were addressed by replacing annealing at 900℃ with 1 min dry oxidation and 20 mins annealing at 1100℃ to change the grain size on 30 nm thick SiNW which reduces the thickness of the

SiNW down to 20 nm and also reduces the dopant concentration down to $7 \times 10^17 atoms/cm^3$. However, this change induces leakage problems from the buried nitride which was found to be due to grains dislocations in nitride/silicon interface layer mainly due to difference in thermal expansion co-efficient between nitride and bulk silicon substrate. This problem was overcome by adding 30 nm of dry oxide which is viscous at high temperature and reduces the dislocation in nitride layer. At the same time the metallization of electrodes was changed from Cr and Au to TiW and Au adjust the problem of disconnection between source and drain of SiNW after contact annealing step which was happening due to diffusion of Au through Cr and forming silicide with polysilicon. After electrical characterization the sensitivity of the SiNW was improved significantly and complete depletion of the SiNW was possible at very low back gate voltage. Moreover, the electrical characteristics of these SiNW Bio-FET was found to be similar to the one's produced by Lieber's research group which enhances the possibilities of using this device as a biosensor element in POC setup. The pH sensing experiments were made by using the devices made by 3rd generation process but due to leakage of current through SiNW into liquid the measurements were not good. This is due to bad coverage of native oxide on top of SiNW which was improved by depositing 5 nm of Al_2O_3 on top of SiNW soon after patterning. The device testing is under progress.

To integrate the SiNW Bio-FET device with microfluidic system, polyimide material has been investigated as a possible candidate to form microfluidic channel on top of SiNW. A fabrication process was developed and etching parameters were optimized to form PI microfluidic channel on top of SiNW. The possibility of forming closed-channel microfluidics was also studied by optimizing the bonding parameters of PI-PI and PI-glass on the wafer level. The strength of the bonding was tested using hydrodynamic focusing and pressure burst tests. The bonding of the SiNW to PI was also done by using the optimized bonding parameters where the holes for inlet and openings of the contact pads were made using laser micromachining on the PI coated glass wafer.

Base on the electrical characterization and bio sensing experiments results and comparing them with the research work already done, it can be concluded that the SiNW fabrication process developed in this project has a potential to be used in industry to produce low cost Bio-FET devices that will enable its availability in a POC devices.

By improving the functionalization protocol with the feature of in-flow functionalization of SiNW using microfluidics and developing read-out setup with smart phone control system this device can be developed into POC device.

Bibliography

Book Sources

[18] Maria Teresa Giardi, Giuseppina Rea, and Bruno Berra. *Bio-farms for nutraceuticals. Functional food and safety control by biosensors. Preface.* Vol. 698. 2010, pp. vii–viii. ISBN: 9781441973474 (cit. on p. 1).

[19] T.Jorgensen Jan and Winther Henrik. *The key Driver in Personalized Cancer Medicine, Molecular Diagnostics*. Pan Stanford Publishing Pte., USA, 2010. ISBN: 10981424144X (cit. on p. 1).

[26] M.Bujalowski Wlodek. *Spectroscopic Methods and Analysis:Methods and Protocols*. Galveston, TX, USA, 2012, pp. 193–214. ISBN: 9781617798054 (cit. on p. 2).

[65] Jacob Millman and Christos C. Halkias. *Electronic Devices and Circuits*. 1967. ISBN: 0070423806 (cit. on p. 11).

[66] SZE S.M. *Semicondcutor devices, physics and technology*. New York, USA, 1985. ISBN: 0471874248 (cit. on pp. 11, 86, 87).

[67] Donald A. Naemen. *Semiconductor Physics and Devices: Basic Principles*. 2003. ISBN: 0072321075 (cit. on pp. 12, 13).

[68] Jacob H. Masliyah and Subir Bhattacharjee. *ELECTROKINETIC AND COLLOID TRANSPORT PHENOMENA*. 2006. ISBN: 9780471788829 (cit. on pp. 15–17).

[69] Jacob Israelachvili. *Intermolecular and Surface Forces*. 1991, pp. 231–234. ISBN: 0123751810 (cit. on pp. 15–17).

[70] Neil W. Ashcroft and N.David Mermin. *Solid State Physics*. 1981. ISBN: 0030493463 (cit. on p. 18).

Other Sources

[1] Lc C Clark and C Lyons. "Electrode systems for continuous monitoring in cardiovascular surgery". In: *Annals Of The New York Academy Of Sciences* 102.1 (1962), pp. 29–45. ISSN: 00778923. DOI: 10.1111/j.1749-6632.1962.tb13623.x (cit. on p. 1).

[2] Song Hyun Seok and Tai Hyun Park. "Integration of biomolecules and nanomaterials: Towards highly selective and sensitive biosensors". In: *Biotechnology Journal* 6.11 (2011), pp. 1310–1316. ISSN: 18606768. DOI: 10.1002/biot.201100006 (cit. on p. 1).

[3] Jeong Woo Choi et al. "Nanotechnology in biodevices". In: *Journal of Microbiology and Biotechnology* 17.1 (2007), pp. 5–14. ISSN: 10177825 (cit. on p. 1).

[4] Michael Holzinger, Alan Le Goff, and Serge Cosnier. "Nanomaterials for biosensing applications: A Review". In: *Frontiers in Chemistry* 2.August (2014), pp. 1–10. ISSN: 2296-2646. DOI: 10.3389/fchem.2014.00063 (cit. on p. 1).

[5] Kewal K. Jain. "Applications of nanobiotechnology in clinical diagnostics". In: *Clinical Chemistry* 53.11 (2007), pp. 2002–2009. ISSN: 00099147. DOI: 10.1373/clinchem.2007.090795 (cit. on p. 1).

[6] R Seigneuric et al. "From nanotechnology to nanomedicine: applications to cancer research." In: *Current molecular medicine* 10.7 (2010), pp. 640–652. ISSN: 15665240. DOI: 10.2174/156652410792630634 (cit. on p. 1).

[7] S. K. Sahoo, S. Parveen, and J. J. Panda. "The present and future of nanotechnology in human health care". In: *Nanomedicine: Nanotechnology, Biology, and Medicine* 3.1 (2007), pp. 20–31. ISSN: 15499634. DOI: 10.1016/j.nano.2006.11.008 (cit. on p. 1).

[8] Kewal K. Jain. "Nanotechnology in clinical laboratory diagnostics". In: *Clinica Chimica Acta* 358.1-2 (2005), pp. 37–54. ISSN: 00098981. DOI: 10.1016/j.cccn.2005.03.014 (cit. on p. 1).

[9] James F Leary. "Nanotechnology: what is it and why is small so big?" In: *Canadian journal of ophthalmology. Journal canadien d'ophtalmologie* 45.5 (2010), pp. 449–456. ISSN: 0008-4182. DOI: 10.3129/i10-089.
http://dx.doi.org/10.3129/i10-089
(cit. on pp. 1, 2).

[10] Leon M. Bellan, Diana Wu, and Robert S. Langer. "Current trends in nanobiosensor technology". In: *Wiley Interdisciplinary Reviews: Nanomedicine and Nanobiotechnology* 3.3 (2011), pp. 229–246. ISSN: 19395116. DOI: 10.1002/wnan.136 (cit. on p. 1).

[11] Evgenia Baranova et al. "Infectious Diseases and Nanomedicine I". In: 807 (2014), pp. 9–21. DOI: 10.1007/978-81-322-1777-0.
http://link.springer.com/10.1007/978-81-322-1777-0
(cit. on p. 1).

[12] Jianling Wang et al. "Advances in nano-scaled biosensors for biomedical applications." In: *The Analyst* 138.16 (2013), pp. 4427–35. ISSN: 1364-5528. DOI: 10.1039/c3an00438d.
http://www.ncbi.nlm.nih.gov/pubmed/23748648
(cit. on p. 1).

[13] Cangel Pui Yee Chan et al. "Evidence-based point-of-care diagnostics: current status and emerging technologies." In: *Annual review of analytical chemistry (Palo Alto, Calif.)* 6 (2013), pp. 191–211. ISSN: 1936-1335. DOI: 10.1146/annurev-anchem-062012-092641.
http://www.ncbi.nlm.nih.gov/pubmed/23527548
(cit. on p. 1).

[14] David R Walt. "Coatings for medical diagnostics." In: *Medical device technology* 16.4 (2005), p. 52. ISSN: 10486690 (cit. on p. 1).

[15] B. Srinivasan and S. Tung. "Development and Applications of Portable Biosensors". In: *Journal of Laboratory Automation* (2015). ISSN: 2211-0682. DOI: 10.1177/2211068215581349.
http://jla.sagepub.com/lookup/doi/10.1177/2211068215581349
(cit. on pp. 1, 2, 4).

[16] Suveen Kumar et al. "Microfluidic-integrated biosensors: Prospects for point-of-care diagnostics". In: *Biotechnology Journal* 8.11 (2013), pp. 1267–1279. ISSN: 18606768. DOI: 10.1002/biot.201200386 (cit. on pp. 1, 2).

[17] Daniel V Lim et al. "Current and Developing Technologies for Monitoring Agents of Bioterrorism and Biowarfare Current and Developing Technologies for Monitoring Agents of Bioterrorism and Biowarfare". In: 18.4 (2005), pp. 583–607. DOI: 10.1128/CMR.18.4.583 (cit. on pp. 1, 2).

[20] H.Nichols James. "NACB:Laboratory Medicine Practice Guidelines. Evidence-based practice for Point of care testing." In: (2006), pp. 13–17 (cit. on p. 1).

[21] Fernando Patolsky et al. "Electrical detection of single viruses." In: *Proceedings of the National Academy of Sciences of the United States of America* 101.39 (Sept. 2004), pp. 14017–22. ISSN: 0027-8424. DOI: 10.1073/pnas.0406159101.
http://www.pubmedcentral.nih.gov/articlerender.fcgi?artid=521090%5C&tool=pmcentrez%5C&rendertype=abstract
(cit. on pp. 1, 5).

[22] Frederick L. Kiechle and Carol a. Holland. "Point-of-Care Testing and Molecular Diagnostics: Miniaturization Required". In: *Clinics in Laboratory Medicine* 29.3 (2009), pp. 555–560. ISSN: 02722712. DOI: 10.1016/j.cll.2009.06.013 (cit. on p. 1).

[23] Vladimir Gubala et al. "Point of care diagnostics: Status and future". In: *Analytical Chemistry* 84.2 (2012), pp. 487–515. ISSN: 00032700. DOI: 10.1021/ac2030199 (cit. on p. 1).

[24] Kensall D. Wise. "Integrated sensors, MEMS, and microsystems: Reflections on a fantastic voyage". In: *Sensors and Actuators, A: Physical* 136.1 (2007), pp. 39–50. ISSN: 09244247. DOI: 10.1016/j.sna.2007.02.013 (cit. on p. 2).

[25] Luc Gervais, Nico De Rooij, and Emmanuel Delamarche. "Microfluidic chips for point-of-care immunodiagnostics". In: *Advanced Materials* 23.24 (2011). ISSN: 09359648. DOI: 10.1002/adma.201100464 (cit. on p. 2).

[27] Brian B. Haab. "Methods and applications of antibody microarrays in cancer research". In: *Proteomics* 3.11 (2003), pp. 2116–2122. ISSN: 16159853. DOI: 10.1002/pmic.200300595 (cit. on p. 3).

[28] Tza-Huei Wang Tza-Huei Wang, S. Masset, and Chih-Ming Ho Chih-Ming Ho. "A zepto mole DNA micro sensor". In: *Technical Digest. MEMS 2001. 14th IEEE International Conference on Micro Electro Mechanical Systems (Cat. No.01CH37090)* (2001), pp. 10–13. ISSN: 1084-6999. DOI: 10.1109/MEMSYS.2001.906570 (cit. on p. 3).

[29] Bastian E. Rapp, Friederike J. Gruhl, and Kerstin Länge. "Biosensors with label-free detection designed for diagnostic applications". In: *Analytical and Bioanalytical Chemistry* 398.6 (2010), pp. 2403–2412. ISSN: 16182642. DOI: 10.1007/s00216-010-3906-2 (cit. on p. 3).

[30] Heather K Hunt and Andrea M Armani. "Label-free biological and chemical sensors." In: *Nanoscale* 2.9 (2010), pp. 1544–1559. ISSN: 2040-3364. DOI: 10.1039/c0nr00201a (cit. on pp. 3, 4).

[31] Jonathan.S Daniels and Nader Pourmand. "Label-Free Impedance Biosensors: Opportunities and Challenges". In: *National Institute of Health* 29.6 (2012), pp. 997–1003. ISSN: 15378276. DOI: 10.1016/j.biotechadv.2011.08.021.Secreted. arXiv: NIHMS150003 (cit. on pp. 3, 4).

[32] Company Website. *Biosensing Instrument*. 2015 (accessed May 16, 2015). http://www.biosensingusa.com/Application103.html (cit. on pp. 3, 4).

[33] K. Bizet, C. Gabrielli, and H. Perrot. "Biosensors based on piezolectric transducers". In: *Analusis* 27.7 (1999), pp. 609–616. ISSN: 0365-4877. DOI: 10.1051/analusis:1999270609 (cit. on p. 4).

[34] Yeison Montagut et al. "QCM Technology in Biosensors". In: *Biosensors - Emerging Materials and Applications* (2011), p. 630. http://www.intechopen.com/books/biosensors-emerging-materials-and-applications/qcm-technology-in-biosensors (cit. on p. 4).

[35] M a Cooper et al. "Direct and sensitive detection of a human virus by rupture event scanning." In: *Nature biotechnology* 19.9 (2001), pp. 833–837. ISSN: 1087-0156. DOI: 10.1038/nbt0901-833 (cit. on p. 4).

[36] Kyo Seon Hwang et al. "Micro- and nanocantilever devices and systems for biomolecule detection." In: *Annual review of analytical chemistry (Palo Alto, Calif.)* 2 (2009), pp. 77–98. ISSN: 1936-1327. DOI: 10.1146/annurev-anchem-060908-155232 (cit. on p. 4).

[37] Christiane Ziegler. "Cantilever-based biosensors". In: *Analytical and Bioanalytical Chemistry* 379.7-8 (2004), pp. 946–959. ISSN: 16182642. DOI: 10.1007/s00216-004-2694-y (cit. on p. 4).

[38] a. Gupta, D. Akin, and R. Bashir. "Single virus particle mass detection using microresonators with nanoscale thickness". In: *Applied Physics Letters* 84.11 (2004), pp. 1976–1978. ISSN: 00036951. DOI: 10.1063/1.1667011 (cit. on p. 4).

[39] Thomas P Burg et al. "Weighing of biomolecules, single cells and single nanoparticles in fluid." In: *Nature* 446.7139 (2007), pp. 1066–1069. ISSN: 0028-0836. DOI: 10.1038/nature05741 (cit. on p. 4).

[40] Hitoshi Ohnuki et al. "Incorporation of glucose oxidase into Langmuir-Blodgett films based on Prussian blue applied to amperometric glucose biosensor." In: *Langmuir : the ACS journal of surfaces and colloids* 23.8 (2007), pp. 4675–4681. ISSN: 0743-7463. DOI: 10.1021/la063175g (cit. on p. 4).

[41] Guodong Liu and Yuehe Lin. "Biosensor based on self-assembling acetylcholinesterase on carbon nanotubes for flow injection/amperometric detection of organophosphate pesticides and nerve agents". In: *Analytical Chemistry* 78.3 (2006), pp. 835–843. ISSN: 00032700. DOI: 10.1021/ac051559q (cit. on p. 4).

[42] Izabela Sokal et al. "NIH Public Access". In: 29.7 (2012), pp. 625–634. DOI: 10.1038/nbt.1900.A (cit. on p. 4).

[43] Y Cui et al. "Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species." In: *Science (New York, N.Y.)* 293.5533 (2001), pp. 1289–1292. ISSN: 0036-8075. DOI: 10.1126/science.1062711 (cit. on pp. 5, 6).

[44] Jong-in Hahm and Charles M. Lieber. "Direct Ultrasensitive Electrical Detection of DNA and DNA Sequence Variations Using Nanowire Nanosensors". In: *Nano Letters* 4.1 (Jan. 2004), pp. 51–54. ISSN: 1530-6984. DOI: 10.1021/nl034853b.
http://pubs.acs.org/doi/abs/10.1021/nl034853b
(cit. on p. 5).

[45] Gengfeng Zheng et al. "Multiplexed electrical detection of cancer markers with nanowire sensor arrays." In: *Nature biotechnology* 23.10 (Oct. 2005), pp. 1294–301. ISSN: 1087-0156. DOI: 10.1038/nbt1138.
http://www.ncbi.nlm.nih.gov/pubmed/16170313
(cit. on pp. 5, 27).

[46] Eric Stern et al. "Label-free immunodetection with CMOS-compatible semiconducting nanowires." In: *Nature* 445.7127 (2007), pp. 519–522. ISSN: 0028-0836. DOI: 10.1038/nature05498 (cit. on p. 5).

[47] X.T. Vu et al. "Fabrication and application of silicon nanowire transistor arrays for biomolecular detection". In: *Sensors and Actuators B: Chemical* 144.2 (Feb. 2010), pp. 354–360. ISSN: 09254005. DOI: 10.1016/j.snb.2008.11.048.
http://linkinghub.elsevier.com/retrieve/pii/S0925400508007983
(cit. on pp. 5, 25–27).

[48] O Knopfmacher et al. "Nernst limit in dual-gated Si-nanowire FET sensors." In: *Nano letters* 10.6 (June 2010), pp. 2268–74. ISSN: 1530-6992. DOI: 10.1021/nl100892y.
http://www.ncbi.nlm.nih.gov/pubmed/20499926
(cit. on pp. 5, 25–27).

[49] Niklas Elfström, Amelie Eriksson Karlström, and Jan Linnros. "Silicon nanoribbons for electrical detection of biomolecules." In: *Nano letters* 8.3 (Mar. 2008), pp. 945–9. ISSN: 1530-6984. DOI: 10.1021/nl080094r.
http://www.ncbi.nlm.nih.gov/pubmed/18266330
(cit. on pp. 5, 25–27).

[50] Aleksandar Vacic et al. "Multiplexed SOI BioFETs." In: *Biosensors & bioelectronics* 28.1 (Oct. 2011), pp. 239–42. ISSN: 1873-4235. DOI: 10.1016/j.bios.2011.07.025.
http://www.pubmedcentral.nih.gov/articlerender.fcgi?artid=3235496%5C&tool=pmcentrez%5C&rendertype=abstract
(cit. on p. 5).

[51] Inkyu Park et al. "Top-down fabricated silicon nanowire sensors for real-time chemical detection." In: *Nanotechnology* 21.1 (Jan. 2010), p. 015501. ISSN: 1361-6528. DOI: 10.1088/0957-4484/21/1/015501.
http://www.ncbi.nlm.nih.gov/pubmed/19946164
(cit. on pp. 5, 7, 8, 25, 27).

[52] Na Lu et al. "CMOS-compatible silicon nanowire field-effect transistors for ultrasensitive and label-free microRNAs sensing." In: *Small (Weinheim an der Bergstrasse, Germany)* 10.10 (May 2014), pp. 2022–8. ISSN: 1613-6829. DOI: 10.1002/smll.201302990.
http://www.ncbi.nlm.nih.gov/pubmed/24574202
(cit. on p. 5).

[53] Jay Huiyi Chua et al. "Label-free electrical detection of cardiac biomarker with complementary metal-oxide semiconductor-compatible silicon nanowire sensor arrays." In: *Analytical chemistry* 81.15 (Aug. 2009), pp. 6266–71. ISSN: 1520-6882. DOI: 10.1021/ac901157x.
http://www.ncbi.nlm.nih.gov/pubmed/20337397
(cit. on p. 5).

[54] Guo-Jun Zhang et al. "An integrated chip for rapid, sensitive, and multiplexed detection of cardiac biomarkers from fingerprick blood." In: *Biosensors & bioelectronics* 28.1 (Oct. 2011), pp. 459–63. ISSN: 1873-4235. DOI: 10.1016/j.bios.2011.07.007.
http://www.ncbi.nlm.nih.gov/pubmed/21807497
(cit. on p. 5).

[55] Guo-Jun Zhang et al. "Silicon nanowire biosensor for highly sensitive and rapid detection of Dengue virus". In: *Sensors and Actuators B: Chemical* 146.1 (Apr. 2010), pp. 138–144. ISSN: 09254005. DOI: 10.1016/j.snb.2010.02.021.
http://linkinghub.elsevier.com/retrieve/pii/S0925400510001255
(cit. on pp. 5, 25, 27).

[56] Hien Duy Tong et al. "Novel Top-Down Wafer-Scale Fabrication of Single Crystal Silicon Nanowires 2009". In: (2009) (cit. on pp. 5, 25–27).

[57] G. Jayakumar et al. "Silicon nanowires integrated with CMOS circuits for biosensing application". In: *Solid-State Electronics* 98 (Aug. 2014), pp. 26–31. ISSN: 00381101. DOI: 10.1016/j.sse.2014.04.005.
http://linkinghub.elsevier.com/retrieve/pii/S0038110114000537
(cit. on p. 5).

[58] Mohammad M a Hakim et al. "Thin film polycrystalline silicon nanowire biosensors." In: *Nano letters* 12.4 (Apr. 2012), pp. 1868–72. ISSN: 1530-6992. DOI: 10.1021/nl2042276.
http://www.ncbi.nlm.nih.gov/pubmed/22432636
(cit. on pp. 5, 8, 25, 26).

[59] Guo-Jun Zhang et al. "Highly sensitive measurements of PNA-DNA hybridization using oxide-etched silicon nanowire biosensors." In: *Biosensors & bioelectronics* 23.11 (June 2008), pp. 1701–7. ISSN: 0956-5663. DOI: 10.1016/j.bios.2008.02.006.
http://www.ncbi.nlm.nih.gov/pubmed/18356037
(cit. on p. 5).

[60] a Agarwal et al. "Silicon nanowire sensor array using top–down CMOS technology". In: *Sensors and Actuators A: Physical* 145-146 (July 2008), pp. 207–213. ISSN: 09244247. DOI: 10.1016/j.sna.2007.12.019.
http://dx.doi.org/10.1016/j.sna.2007.12.019
(cit. on pp. 5, 25–27).

[61] Min-Cheng Chen et al. "A CMOS-compatible poly-Si nanowire device with hybrid sensor/memory characteristics for System-on-Chip applications." In: *Sensors (Basel, Switzerland)* 12.4 (Jan. 2012), pp. 3952–63. ISSN: 1424-8220. DOI: 10.3390/s120403952.
http://www.pubmedcentral.nih.gov/articlerender.fcgi?artid=3355393%5C&tool=pmcentrez%5C&rendertype=abstract
(cit. on pp. 5, 25).

[62] Guo-Jun Zhang et al. "DNA sensing by silicon nanowire: charge layer distance dependence." In: *Nano letters* 8.4 (Apr. 2008), pp. 1066–70. ISSN: 1530-6984. DOI: 10.1021/nl0729911.
http://www.ncbi.nlm.nih.gov/pubmed/18311939
(cit. on p. 5).

[63] Fernando Patolsky, Gengfeng Zheng, and Charles M Lieber. "Fabrication of silicon nanowire devices for ultrasensitive, label-free, real-time detection of biological and chemical species." In: *Nature protocols* 1.4 (2006), pp. 1711–1724. ISSN: 1754-2189. DOI: 10.1038/nprot.2006.227 (cit. on pp. 7, 27, 62, 63).

[64] Xuan Thang Vu et al. "Top-down processed silicon nanowire transistor arrays for biosensing". In: *Physica Status Solidi (a)* 206.3 (Mar. 2009), pp. 426–434. ISSN: 18626300. DOI: 10.1002/pssa.200880475.
http://doi.wiley.com/10.1002/pssa.200880475
(cit. on pp. 8, 25–27).

[71] Martin Hedegard sørensen, Niels Asger Mortensen, and Mads Brandbyge. "Screening model for nanowire surface-charge sensors in liquid". In: *Applied Physics Letters* 91.10 (2007), pp. 1–3. ISSN: 00036951. DOI: 10.1063/1.2779930. eprint:
0708.2001
(cit. on p. 18).

[72] Xuan P a Gao, Gengfeng Zheng, and Charles M Lieber. "Subthreshold regime has the optimal sensitivity for nanowire FET biosensors." In: *Nano letters* 10.2 (Feb. 2010), pp. 547–52. ISSN: 1530-6992. DOI: 10.1021/nl9034219. http://www.pubmedcentral.nih.gov/articlerender.fcgi?artid=2820132%5C&tool=pmcentrez%5C&rendertype=abstract
(cit. on pp. 19, 74).

[73] Cheng-Yun Hsiao et al. "Novel poly-silicon nanowire field effect transistor for biosensing application." In: *Biosensors & bioelectronics* 24.5 (Jan. 2009), pp. 1223–9. ISSN: 1873-4235. DOI: 10.1016/j.bios.2008.07.032. http://www.ncbi.nlm.nih.gov/pubmed/18760914
(cit. on p. 25).

[74] Chih-Heng Lin et al. "Poly-silicon nanowire field-effect transistor for ultrasensitive and label-free detection of pathogenic avian influenza DNA." In: *Biosensors & bioelectronics* 24.10 (June 2009), pp. 3019–24. ISSN: 1873-4235. DOI: 10.1016/j.bios.2009.03.014. http://www.ncbi.nlm.nih.gov/pubmed/19362813
(cit. on p. 25).

[75] Chih-Heng Lin et al. "Ultrasensitive detection of dopamine using a polysilicon nanowire field-effect transistor." In: *Chemical communications (Cambridge, England)* 44 (Nov. 2008), pp. 5749–51. ISSN: 1364-548X. DOI: 10.1039/b812968a. http://www.ncbi.nlm.nih.gov/pubmed/19009069
(cit. on p. 25).

[76] Eric Stern et al. "Importance of the Debye Screening Length on Nanowire Field Effect Transistor Sensors". In: 1 (2007), pp. –4 (cit. on pp. 25, 26).

[77] Eric Stern et al. "NIH Public Access". In: 7.11 (2009), pp. 3405–3409. DOI: 10.1021/nl071792z.Importance (cit. on pp. 25, 26).

[78] O. Knopfmacher et al. "Dual Gated Silicon Nanowire Field Effect Transistors". In: *Procedia Chemistry* 1.1 (Sept. 2009), pp. 678–681. DOI: 10.1016/j.proche.2009.07.169. http://linkinghub.elsevier.com/retrieve/pii/S1876619609001703
(cit. on p. 26).

[79] Jean-Pierre Colinge et al. "Nanowire transistors without junctions." In: *Nature nanotechnology* 5.3 (2010), pp. 225–229. ISSN: 1748-3387. DOI: 10.1038/nnano.2010.15. http://dx.doi.org/10.1038/nnano.2010.15
(cit. on pp. 26, 53).

[80] J P Gambino and E G Colgan. "Silicides and ohmic contacts". In: 52 (1998), pp. 99–146 (cit. on pp. 26, 53).

[81] Yuri L Bunimovich et al. "Quantitative real-time measurements of DNA hybridization with alkylated nonoxidized silicon nanowires in electrolyte solution." In: *Journal of the American Chemical Society* 128.50 (Dec. 2006), pp. 16323–31. ISSN: 0002-7863. DOI: 10.1021/ja065923u. http://www.pubmedcentral.nih.gov/articlerender.fcgi?artid=3695614%5C&tool=pmcentrez%5C&rendertype=abstract
(cit. on p. 27).

[82] H C Shin and Chenming Hu. "Thin gate oxide damage due to plasma processing". In: *Semiconductor Science and Technology* 11.4 (1999), pp. 463–473. ISSN: 0268-1242. DOI: 10.1088/0268-1242/11/4/002 (cit. on p. 30).

[83] a Belkacem et al. "Electronic Defects Induced in Silicon by SF 6 Plasma Etching". In: *Materials Science* 4 (1989), pp. 451–455 (cit. on p. 30).

[84] D Misra and E L Heasell. "Electrical damage to silicon devices due to reactive ion etching". In: *Semiconductor Science and Technology* 5.3 (1999), pp. 229–236. ISSN: 0268-1242. DOI: 10.1088/0268-1242/5/3/008 (cit. on p. 30).

[85] Stefan Chisca et al. "Dielectric and conduction properties of polyimide films". In: *CAS 2011 Proceedings (2011 International Semiconductor Conference)* (Oct. 2011), pp. 253–256. DOI: 10.1109/SMICND.2011.6095784. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6095784 (cit. on pp. 30, 38).

[86] Azeem Zulfiqar et al. "Fabrication of polyimide based microfluidic channels for biosensor devices". In: *Journal of Micromechanics and Microengineering* 25.3 (2015), p. 035022. ISSN: 0960-1317. DOI: 10.1088/0960-1317/25/3/035022. http://stacks.iop.org/0960-1317/25/i=3/a=035022?key=crossref.7b9a026efab87e9e5922af54727f3ea4 (cit. on pp. 30, 38).

[87] Martina Bachlechner et al. "Dislocation Emission at the Silicon/Silicon Nitride Interface: A Million Atom Molecular Dynamics Simulation on Parallel Computers". In: *Physical Review Letters* 84.2 (2000), pp. 322–325. ISSN: 0031-9007. DOI: 10.1103/PhysRevLett.84.322 (cit. on pp. 34, 59).

[88] Takashi Noguchi, Hisao Hayashi, and Takefumi Ohshima. " Grain Growth and Conductive Characteristics of Super Thin Polysilicon Films by Oxidation ". In: *Japanese Journal of Applied Physics* 24.Part 2, No. 6 (1985), pp. L434–L436. ISSN: 0021-4922. DOI: 10.1143/JJAP.24.L434 (cit. on p. 34).

[89] A. Ait-Kakia and D. Rechem. In: *THE EUROPEAN PHYSICAL JOURNAL APPLIED PHYSICS* (2004), pp. 77–84 (cit. on p. 34).

[90] H Cerva and H Oppolzer. *Microstructure and interfaces of polysilicon in Integrated Circuits*. 1989 (cit. on p. 34).

[91] J. R. Rairden, C. a. Neugebauer, and R. a. Sigsbee. "Interdiffusion in thin conductor films - chromium/gold, nickel/gold and chromium silicide/gold". In: *Metallurgical Transactions* 2.3 (1971), pp. 719–722. ISSN: 0026086X. DOI: 10.1007/BF02662726 (cit. on p. 35).

[92] Jindong Wang et al. "Preparation of silicon nanowires by in situ doping and their electrical properties". In: *Colloids and Surfaces A: Physicochemical and Engineering Aspects* 450 (May 2014), pp. 156–160. ISSN: 09277757. DOI: 10.1016/j.colsurfa.2014.03.028. http://linkinghub.elsevier.com/retrieve/pii/S0927775714002507 (cit. on p. 35).

[93] S Metz, R Holzer, and P Renaud. "Polyimide-based microfluidic devices." In: *Lab on a chip* 1.1 (Sept. 2001), pp. 29–34. ISSN: 1473-0197. DOI: 10.1039/b103896f.
http://www.ncbi.nlm.nih.gov/pubmed/15100886
(cit. on pp. 37, 38, 45).

[94] Jessamine Ng Lee, Cheolmin Park, and George M Whitesides. "Solvent compatibility of poly(dimethylsiloxane)-based microfluidic devices." In: *Analytical chemistry* 75.23 (Dec. 2003), pp. 6544–54. ISSN: 0003-2700. DOI: 10.1021/ac0346712.
http://www.ncbi.nlm.nih.gov/pubmed/14640726
(cit. on p. 38).

[95] The Chemical et al. "Resin Codes :" in: () (cit. on p. 38).

[96] Letizia Amato et al. "Fabrication of high-aspect ratio SU-8 micropillar arrays". In: *Microelectronic Engineering* 98 (Oct. 2012), pp. 483–487. ISSN: 01679317. DOI: 10.1016/j.mee.2012.07.092.
http://linkinghub.elsevier.com/retrieve/pii/S0167931712003747
(cit. on p. 38).

[97] S Metz et al. "Flexible polyimide probes with microelectrodes and embedded microfluidic channels for simultaneous drug delivery and multi-channel monitoring of bioelectric activity." In: *Biosensors & bioelectronics* 19.10 (May 2004), pp. 1309–18. ISSN: 0956-5663. DOI: 10.1016/j.bios.2003.11.021.
http://www.ncbi.nlm.nih.gov/pubmed/15046764
(cit. on p. 38).

[98] T. N. T. Nguyen and N.-E. Lee. "Deep Reactive Ion Etching of Polyimide for Microfluidic Applications". In: *Journal of the Korean Physical Society* 51.3 (Sept. 2007), p. 984. ISSN: 0374-4884. DOI: 10.3938/jkps.51.984.
http://www.kps.or.kr/jkps/abstract%5C_view.asp?articleuid=A8A3FF79-647E-4A84-AA25-48C2D0B0BF1B
(cit. on pp. 38, 40).

[99] Sung-Won Youn et al. "Fabrication of micro mold for hot-embossing of polyimide microfluidic platform by using electron beam lithography combined with inductively coupled plasma". In: *Microelectronic Engineering* 85.5-6 (May 2008), pp. 918–921. ISSN: 01679317. DOI: 10.1016/j.mee.2008.01.017.
http://linkinghub.elsevier.com/retrieve/pii/S0167931708000488
(cit. on p. 38).

[100] T. Walewyns et al. "<title>Fabrication of a miniaturized ionization gas sensor with polyimide spacer</title>". In: 8066 (May 2011). Ed. by Ulrich Schmid, José Luis Sánchez-Rojas, and Monika Leester-Schaedel, DOI: 10.1117/12.886759.
http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=1351086
(cit. on pp. 38, 40).

[101] Kirt R Williams et al. "Etch Rates for Micromachining Processing — Part II". In: (2003) (cit. on pp. 38, 89).

[102] A Crockett, M Almoustafa, and W Vanderlinde. "Plasma Delayering of Integrated Circuits". In: () (cit. on p. 40).

[103] M. Huh et al. "Galvanic Corrosion during Processing of Polysilicon Microelectromechanical Systems". In: *Journal of The Electrochemical Society* 153.7 (2006), G644. ISSN: 00134651. DOI: 10.1149/1.2199139 (cit. on p. 55).

[104] L. Torcheux. "Electrochemical Coupling Effects on the Corrosion of Silicon Samples in HF Solutions". In: *Journal of The Electrochemical Society* 142.6 (1995), p. 2037. ISSN: 00134651. DOI: 10.1149/1.2044237 (cit. on p. 55).

[105] John Y W Seto. "The electrical properties of polycrystalline silicon films". In: *Journal of Applied Physics* 46.12 (1975), pp. 5247–5254. ISSN: 00218979. DOI: 10.1063/1.321593 (cit. on pp. 57, 58).

[106] D.P. Joshi and R.S. Srivastava. "Mobility and carrier concentration in polycrystalline silicon". In: *Solar Cells* 12.3 (1984), pp. 337–344. ISSN: 03796787. DOI: 10.1016/0379-6787(84)90112-1 (cit. on p. 58).

[107] P Jeanjean et al. "Dopant activation and Hall mobility in B- and As-implanted polysilicon films after rapid or conventional thermal annealing". In: *Semiconductor Science and Technology* 6.12 (1999), pp. 1130–1134. ISSN: 0268-1242. DOI: 10.1088/0268-1242/6/12/005 (cit. on p. 85).

[108] F. Lanzerath et al. "Boron activation and diffusion in silicon and strained silicon-on-insulator by rapid thermal and flash lamp annealings". In: *Journal of Applied Physics* 104.4 (2008). ISSN: 00218979. DOI: 10.1063/1.2968462 (cit. on p. 85).

[109] M. Y. L. Jung et al. "Ramp-Rate Effects on Transient Enhanced Diffusion and Dopant Activation". In: *Journal of The Electrochemical Society* 150.12 (2003), G838. ISSN: 00134651. DOI: 10.1149/1.1627354 (cit. on p. 85).

Appendix A

Publications

A.1 Publications

- Fabrication of polyimide based microfluidic channels for biosensor devices, Azeem Zulfiqar, Andrea Pfreundt, Winnie Edith Svendsen and Maria Dimaki,Journal of Micromechanics and Microengineering

- Nanoscaled Biological Gated Field Effect Transistors for Cytogenetic Analysis, D. Kwasny, M. Dimaki, K. B. Andersen, A. Zulfiqar, Z. Tümer and W. E. Svendsen, Proceedings of the 9th IEEE International Conference on Nano/Micro Engineered and Molecular Systems April 13-16, 2014, Hawaii, USA

- In-situ doped junctionless polysilicon nanowires field effect transistors for low-cost biosensors. (manuscript in preparation)

A.2 Conference Presentation

- Poster presentation: WAM-NANO 2012, Barcelona, Spain, title: Lab-on-Chip Silicon nanowire biosensors for biomedical applications,June 11-12 2012

- Oral Talk: Thematic days on "Semiconductor Nanowires Based Sensors" of the GDR "Semiconductor Nanowires and Nanotubes" in Rennes France November 13-14, 2012

- Poster Presentation: Gordon Research Conference on Microfluidics, Physics and Chemistry of, title: Translating silicon nanowire BioFET sensor-technology to embedded point-of-care medical diagnostics, June 9-14, 2013

- Poster presentation (co-author presented by Andrea Pfreundt): Lab-on-a-Chip European Congress, 2014, Berlin, title: A novel single-step, multipoint calibration method for instrumented Lab-on-Chip systems

- Poster presentation (co-author presented by François Patou): 24th Anniversary World Congress on Biosensors, 2014, Melbourne, title: A flexible mobile-device biosensing instrumentation platform for point-of-care medical diagnostics applications

- Poster presentation: Materials Research Society Annual Meeting 30.11.2014 to 05.12.2014,title Fabrication and characterization of in-situ doped polysilicon nanowire junctionless field effect transistors for low cost biosensor applications

Appendix B

Process Sequence

SiNW Processs Sequence				
Step	Process	Equipment	Notes	Time
0	Substrate selection		Double side polished p-type wafer, thickness of substrate=350 μm, crystal orientation <100>, 1-20 Ω-cm,	
1	Clean Wafer	RCA bath		
1.2	Grow 30 nm oxide	Dry oxidation	Phophor-Drive-in furnace	Dry oxidation 1100 C	7 mins
1.3	Grow 50 nm silicon nitride	LPCVD Si3N4	6' furnace LPCVD Si3N4	Recipe '4 Nitdan'	20 mins
1.4	Deposit 30 nm polysilicon (boron doped)	LPCVD Polysilicon	4' Polysilicon furnace	Recipe 'polybor'	3 min 30 sec
1.5	Dry oxidation	Oxidation and Annealing	Anneal Oxide C1 furnace	1 min oxidation using recipe dry 1100C with 20 min annealing time	1 min
1.6	Etch away all layers from backside	Dry etching	DRIE Pegeasus	Batch Recipe 'SiNW Etch'	5 min
1.7	Remove oxide from front	BHF with wetting agent	BHF with wet agent		1 min
1.8	Deposit 220 nm Si3N4 mask	PECVD Si3N4	PECVD3	Recipe 'nfsinls'	20 mins 8 secs
2.1	SiNW Pattern	Photoresist primer	HMDS	HMDS oven	30 mins
2.2		Photoresist Spin	SSE Maximus	Recipe "DCH_100mm_AZ5214E_2.2μm'	
2.3		UV lithography	KS Aligner	Mask 1 (NW1), Exposure time 9 sec	
2.4		Development	Developer	Standard developer 80 sec, 5 min rinse, dry	
2.5		Etch Nitride	AOE	Recipe 'nitr_res' at 0C	1 min
2.6		Remove rest of the nitride by wet etch	BHF with wetting agent	5 mins in BHF with wet agent bath, 5 mins rinse in water	10 mins
2.7		Photoresist strip	Acetone Bath	Rough strip 5 mins, Fine strip 5mins , rinse with water	
2.8		Wet etching of polysilicon	KOH3 (4',6') bath	Temperature 15C - 25C. The etch rate will vary. Start with 15 mins of etching time on only 1 wafer first and make inspection in optical microscope if the structures are still there	
2.9		Remove nitride mask	BHF with wetting agent	The etch rate will vary from time to time	8 mins
3.1	ALD Al2O3 deposition	Deposition of 5 nm thick Al2O3 (insulation for SiNW)	ALD Picosun R200	Recipe Al2O3, temperature 300C, TMA cycles 55 (immediately after nitride removal)	20 min
3.2		Photoresist primer	HMDS	HMDS oven	30 mins
3.3		Photoresist Spin	SSE Maximus	Recipe "DCH_100mm_AZ5214E_2.2μm'	
3.4		UV lithography	KS Aligner	Mask 1 (NW1), Exposure time 9 sec	
3.5		Development	Developer	Standard developer 80 sec, 5 min rinse, dry	
3.6		Pattern Al2O3	BHF etch	BHF with wet agent etch for 15 seconds	15 secs
3.7		Photoresist strip	Acetone Bath	Rough strip 5 mins, Fine strip 5mins , rinse with water	

SiNW Processs Sequence					
Step		Process	Equipment	Notes	Time
4.1	Contact Pads Pattern	Photoresist primer	HMDS	HMDS oven	30 mins
4.2	Clean Wafer	Photoresist Spin	SSE Maximus	Recipe '_DCH_100mm_AZ5214E_2.2μm'	
4.3	Grow 30 nm oxide	UV lithography	KS Aligner	Mask 2 (Metal Mask), Exposure time 9 sec	
4.4	Grow 50 nm silicon nitride	Inverse bake	Hot plate next to HMDS Oven	Recipe 110C 180 sec	120 sec
4.5	Deposit 30 nm polysilicon (boron doped)	Flood exposure	KS Aligner	Aligner	30 sec
4.6	Dry oxidation	Development	Developer	Standard developer, 80 sec, rinse 5 min, dry	
4.7	Etch away all layers from backside	Remove oxides from contact areas	BHF with wetting agent	20 secs dip in BHF with wetting agent	20 secs
4.8	Remove oxide from front	RF clean	Wordentec	Process 12. If the reflected power is less than 20W than 30mins30secs clean.If not then 45mins30secs	
4.9	Deposit 220 nm Si3N4 mask	Sputter TiW	Wordentec	Process 8. 30 mins	
4.10	SiNW Pattern Contact Annealing Passivation of contacts	E-beam evaporation Au	Wordentec	Process 7. 150 nm	
4.11		E-beam evaporation Cr/Au	Wordentec	Process 17. Cr=60nm, Au= 100 nm	
4.12		Lift-off	Acetone bath	30 mins in acetone with ultrasonics	30 mins
5.1		Contact annealing	BCB Cure oven	Recipe AzeemPI 350C for 1 hr (immediately after lift-off)	2 hrs
6.1		Photoresist primer	HMDS	HMDS oven	30 mins
6.2		Photoresist Spin	SSE Maximus	Recipe '_DCH_100mm_AZ5214E_2.2μm'	
6.3		UV lithography	KS Aligner	Mask 3 (Microfluidic Mask), Exposure time 9 sec	
6.4		Development	Developer	Standard developer, 80 sec, rinse 5 min, dry	
6.5		Sputter Si3N4 with RF bias and nitrogen	Lesker Sputtering	Recipe ' 'Azeem Source 4 RFbias and N2', Ar 25% N2, 2hrs	7200 secs
6.6		Lift-Off	Acetone bath	30 mins with ultrasonics	30 min
7	Passivation Annealing Chips	Annealing	BCB Cure	Recipe AzeemCT, 450 C for 30 mins	1hr
8	Chips	Dicing			

Appendix C

Recipes

C.1 In-situ doped polysilicon

Temperature [℃]	Pressure [mTorr]	SiH_4 gas flow [sccm]	B_2H_6 gas flow [sccm]
620	200	80	7

Table C.1: Tempress LPCVD polysilicon furnace recipe

C.2 PECVD Si_3N_4

Temperature [℃]	Pressure [mTorr]	SiH_4 gas flow [sccm]	NH_3 gas flow [sccm]	N_2 gas flow [sccm]
300	650	30	30	1470

Table C.2: Oxford Instruments low stress Si_3N_4

Appendix D

Functionalization Protocol

D.1 APTES Functionalization

- (Ideally, surfaces should be cleaned in Piranha solution for 15 min at 105℃, for this refer to the Piranha cleaning protocol, but this can't be done with the SiNW chips.)
- Before functionalization the chips should be cleaned thoroughly in absolute Ethanol and dried in a flow of nitrogen.
- Chips are placed on a microscope slide, facing upwards, and treated with oxygen plasma for 2 minutes (in the Milling lab at maximal power, 0.5mbar oxygen)
- After treatment, place chips immediately into 99% Ethanol to preserve the activated surface.
- Place desiccator on hotplate at 60℃, while flushing Nitrogen through top valve.
- Break off two caps from eppendorf tubes and place into desiccator.
- Clean Hamilton syringes with Chloroform, take 200μL APTES and place into one of the caps
- Do the same with the 50 μL Hünig's base (N,N-Diisopropylethylamine) using the other syringe
- Clean both syringes thoroughly with Chloroform again
- Place chips to be functionalized on a microscope slide and place it into the desiccator next to the caps, keep a low flow of nitrogen.
- Keep in desiccator for 1h.
- Turn up the hotplate to 110℃ and bake for another 5-7 min.
- Store in desiccator under vacuum until further use.

Published by:
DTU Nanotech
Department of Micro- and Nanotechnology
Technical University of Denmark
Ørsteds Plads, building 345B
DK-2800 Kgs. Lyngby